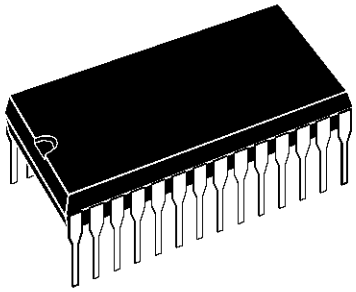
SGS-THOMSON MICROELECTRONICS

ST7294

8-BIT MCU WITH 6K ROM, EEPROM AND 16-BIT TIMER WITH INPUT CAPTURE AND DUAL OUTPUT COMPARE

- 2.5 to 5.5V Supply Operating Range
- 4MHz Maximum Clock Frequency
- Fully Static operation
- -40° to +85°C Operating Temperature Range
- Run, Wait, Stop and RAM Retention modes
- User ROM: 6,144 bytes
- Data RAM: 224 bytes
- EEPROM: 256 bytes
- 28 pin Dual-in-Line and SO plastic packages
- 22 Bidirectional I/O lines
- 6 Interrupt Wake-Up programmable input lines
- 16-bit Timer with Input Capture and dual Output Compare
- 2V RAM Data Retention mode
- Master Reset and Power-On Reset
- Maskable Options for:
  - Input Capture (ICAP) and Output Compare (OCMP) signal pinouts
  - PORT C Wake-Up function
  - PORT A Open-Drain outputs
  - PORTS A and B input Pull-Ups
  - Watchdog Enabled/Disabled following Reset
  - Watchdog Enabled during WAIT mode
- 8-bit Data Manipulation
- 63 Basic Instructions
- 17 main Addressing Modes
- 8x8 Unsigned Multiply instruction
- True Bit Manipulation
- Complete Development Support on PC/DOS Real-Time Emulator
- Full Software Package (Cross-Assembler, Debugger)
- Full Hardware Emulator
- EPROM and OTP support



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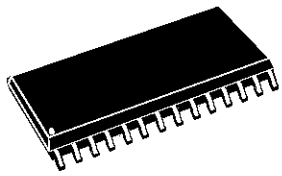
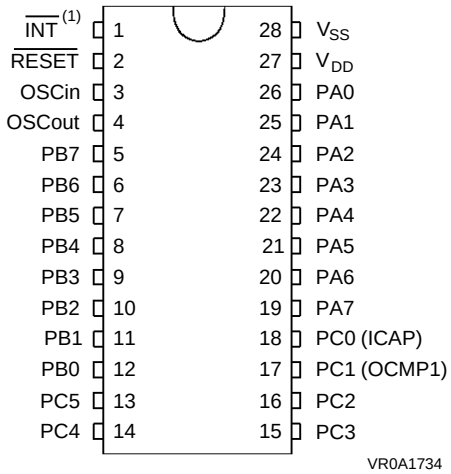


PSO28

(See end of Datasheet for Ordering Information)

Figure 1. Pin Description



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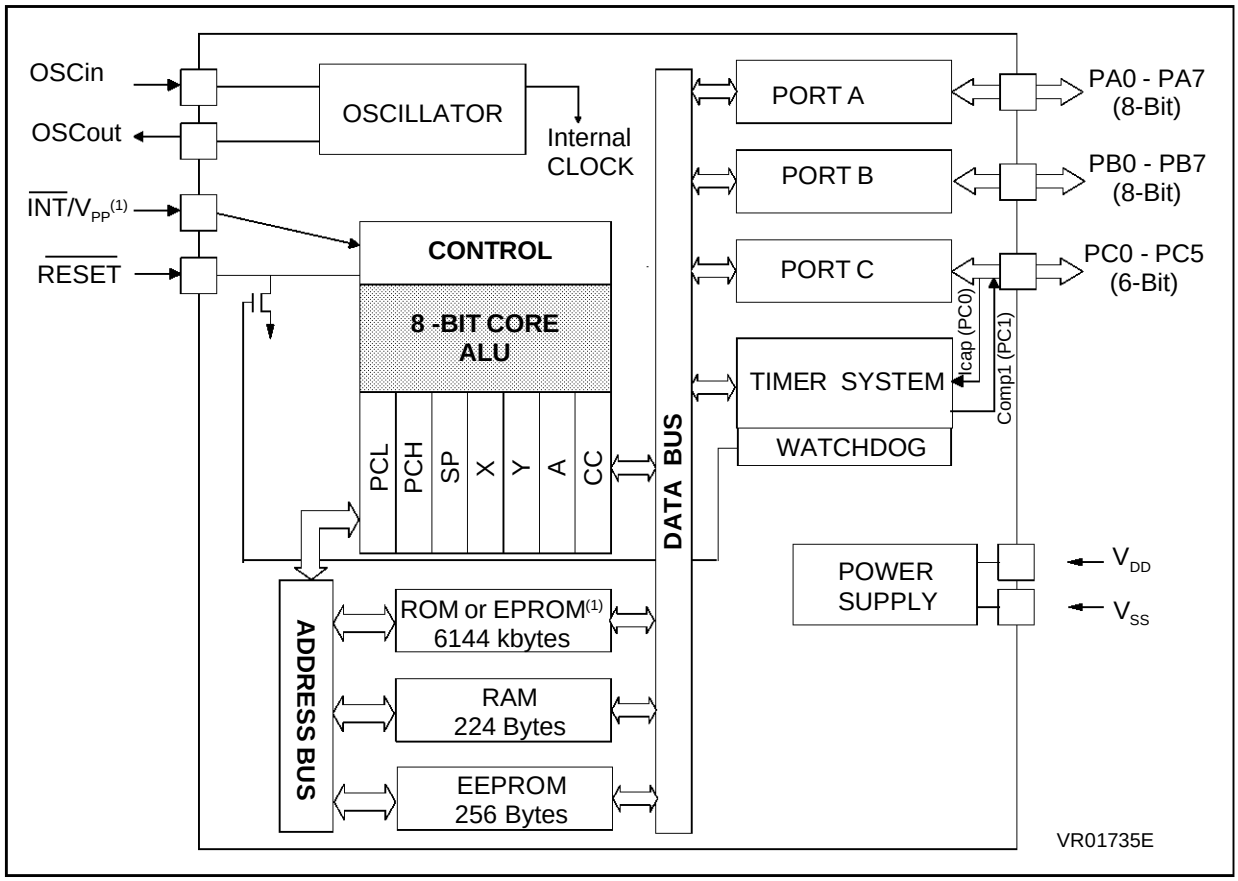
1 GENERAL DESCRIPTION

1.1 INTRODUCTION

The ST7294 HCMOS Microcontroller Unit is a member of the ST7 family of Microcontrollers. The device is based on an industry-standard 8-bit core and features an enhanced instruction set. The CPU may be driven by an external 4MHz clock when the device is operated with a 5V supply, or by a 2MHz clock when operated with a 3V supply. Thanks to the fully static design, operation is possible down to DC. Under software control, the ST7294 may be placed in either WAIT or HALT modes, thus reducing power consumption. The enhanced instruction set and addressing modes afford real programming potential. In addition to standard 8-bit data management, the ST7294 features true bit manipulation, 8x8 unsigned multiplication and indirect addressing modes. The device includes a CPU, ROM, RAM, EEPROM, I/O, an on-chip oscillator and a timer with input capture and dual output compare systems.

Figure 2. ST7294 Block Diagram



Note 1. EPROM version only

1.2 PIN DESCRIPTION

V_{DD} Power supply.

V_{SS} Ground.

OSCin, OSCout Oscillator input and output pins. These pins are usually connected to a parallel resonant crystal or ceramic resonator. An external clock source may also be input via OSCin.

$\overline{\text{RESET}}$ An active-low input signal on this pin forces initialisation of the MCU. This is the highest priority interrupt and it is not maskable. This pin is set to an output-low level following release on the part of the Watchdog. The pin may be used to reset external peripherals.

$\overline{\text{INT}}$ This is the external interrupt input, which may be software-configured in one of four triggering modes.

Caution: *The INT pin is also used to select an internal non-user test mode reserved exclusively for use by* SGS-THOMSON Microelectronics*. This non-user mode is entered on the rising edge of the Reset signal, if:*

– the voltage applied to the INT pin is less than V_{DD} + 0.5V, the device will initialise correctly in User mode;

– if a "high" voltage (typically > V_{DD} + 3V, @ V_{DD} = +5V) is applied to the pin, the device will start in a reserved non-user mode.

Under certain operating conditions apparent device malfunction may be experienced: this may be described as follows:

During the Reset phase, if the V_{DD} supply risetime is slow, the Reset rising edge may occur at a voltage level lower than the minimum allowed voltage of 2.5V. In this case, the "high" voltage which needs to be applied to the INT pin to enter the special mode may be as low as 3.5V, and such a voltage level may be supplied by the external interrupt source, thus provoking an apparent system malfunction.

For this reason it is strongly recommended to manage the INT pin, either by tying it to VDD, if unused, or by connecting it to VDD via a diode, if it is to be used: this will avoid unexpected entry into non-user mode.

ICAP (PC0). Input Capture signal directed to the TIMER system. This pin, according to the chosen mask option, may be defined as the ICAP function input, or as a standard PC0 pin. When the pin is defined as the ICAP input, the internal pull-up resistor is not connected.

OCMP1 (PC1). Output Compare signal originating from the TIMER system. This pin may, depending on the chosen mask option, be defined as the OCMP1 function output (Output Compare 1 of the Timer) or as a standard PC1 pin. When the pin is defined as OCMP1, the internal pull-up resistor is not connected.

PA0-PA7, PB0-PB7, PC0-PC5. These 22 lines are standard I/O lines, programmable as either inputs or outputs.

– PORT A 8 standard I/O lines, bit-programmable via the DDRA and DRA registers. Depending on the chosen mask option, the outputs may be defined as standard push-pull or as open-drain. A further mask option allows a resistor to be added on each line when it is defined as an input.

– PORT B 8 standard I/O lines bit-programmable via the DDRB and DRB registers. A mask option allows a resistor to be added on each line when it is defined as an input.

– PORT C 6 standard I/O lines bit-programmable via the DDRC and DRC registers. Depending on the chosen mask option, these 6 lines can be defined as 6 falling-edge-sensitive interrupt lines, linked to a single interrupt vector, or as 6 standard input ports tied to V_{DD} through an internal pull-up resistor. These negative edge sensitive interrupt lines are capable of waking-up the ST7294 from WAIT or HALT mode. This feature allows one to build low power applications where the ST7294 can be woken-up by a key being pressed.

PIN DESCRIPTION (Continued)

Table 1. ST7294 Pin Configuration

Name	Function	Description	Pin Assignment
$\overline{INT}$	I	Interrupt	1
$\overline{RESET}$	I/O	Reset	2
OSCin	I	Oscillator	3
OSCout	O	Oscillator	4
PB7	I/O	Standard Port (bit programmable)	5
PB6	I/O	Standard Port (bit programmable)	6
PB5	I/O	Standard Port (bit programmable)	7
PB4	I/O	Standard Port (bit programmable)	8
PB3	I/O	Standard Port (bit programmable)	9
PB2	I/O	Standard Port (bit programmable)	10
PB1	I/O	Standard Port (bit programmable)	11
PB0	I/O	Standard Port (bit programmable)	12
PC5	I/O	Standard Port (falling edge interrupt line)	13
PC4	I/O	Standard Port (falling edge interrupt line)	14
PC3	I/O	Standard Port (falling edge interrupt line)	15
PC2	I/O	Standard Port (falling edge interrupt line)	16
PC1 (OCMP1)	I/O	Standard Port (falling edge interrupt line or timer output compare)	17
PC0 (ICAP)	I/O	Standard Port (falling edge interrupt line or timer input capture)	18
PA7	I/O	Standard Port (bit programmable)	19
PA6	I/O	Standard Port (bit programmable)	20
PA5	I/O	Standard Port (bit programmable)	21
PA4	I/O	Standard Port (bit programmable)	22
PA3	I/O	Standard Port (bit programmable)	23
PA2	I/O	Standard Port (bit programmable)	24
PA1	I/O	Standard Port (bit programmable)	25
PA0	I/O	Standard Port (bit programmable)	26
V_{DD}	I/O	Power Supply	27
V_{SS}	I/O	Ground	28

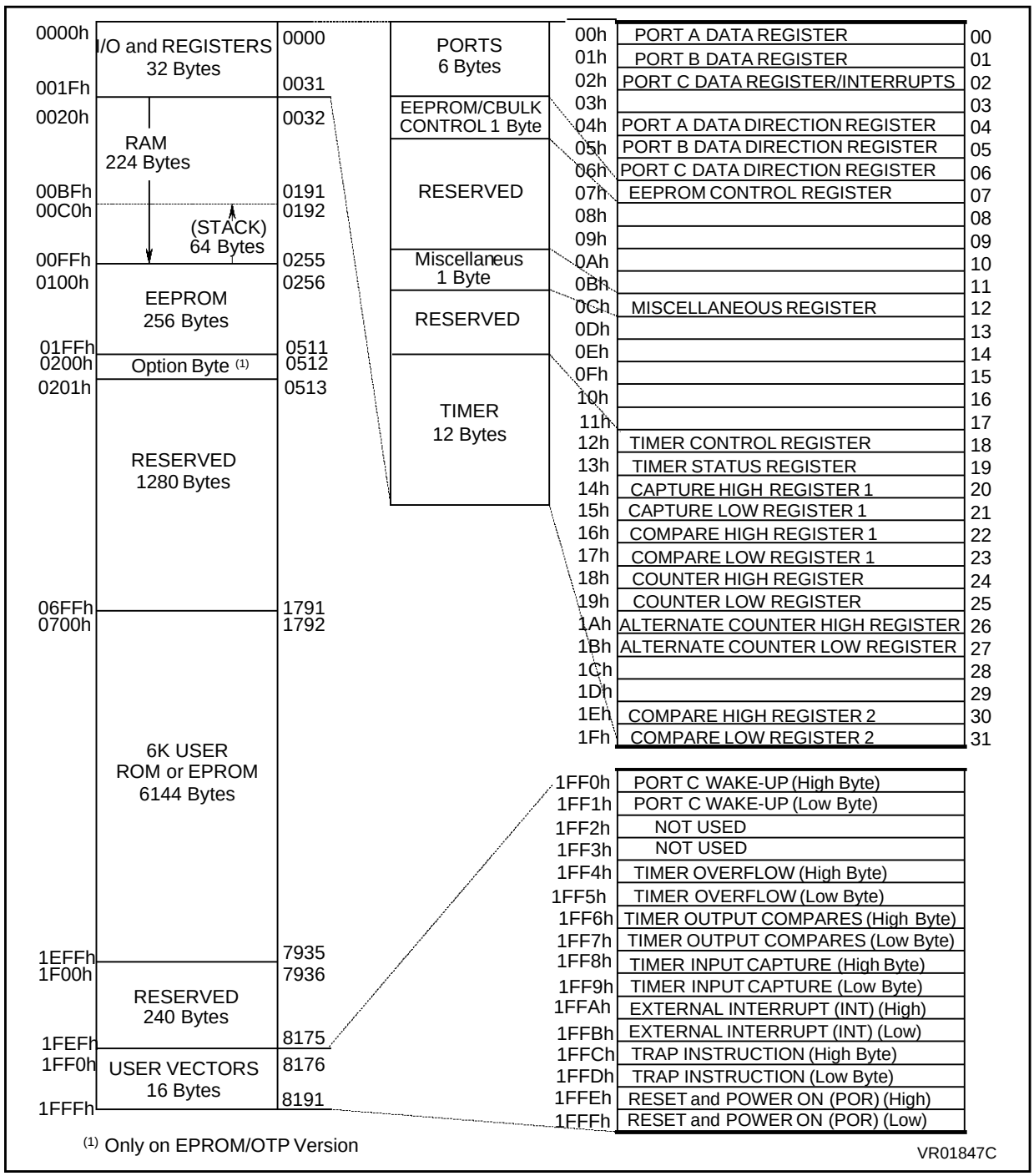
1.3 MEMORY MAP

As shown in Figure 3, the ST7294 is capable of addressing 8,192 bytes of memory and I/O registers, of which 6,612 bytes are user accessible.

The locations consist of 32 bytes of I/O registers (of which only 20 are available), 224 bytes of RAM, 256 bytes of EEPROM and 6 Kbytes of user ROM. The RAM space includes 64 bytes for the stack from 0FFh to 0C0h. Programs that only use a small part of the allocated stack locations for interrupts and/or subroutine stacking purpose can use the remaining bytes as standard RAM locations.

The highest address bytes contain the user-defined reset and interrupt vectors.

Figure 3. ST7294 Memory Map



(1) Only on EPROM/OTP Version

VR01847C

2 CENTRAL PROCESSING UNIT

2.1 INTRODUCTION

The CPU has a full 8-bit architecture. Six internal registers allow efficient 8-bit data manipulations. The CPU is able to execute 74 basic instructions. It features 17 main addressing modes and can address 6 internal registers. It is able to address 6671 bytes of memory and registers with its program counter.

2.2 CPU REGISTERS

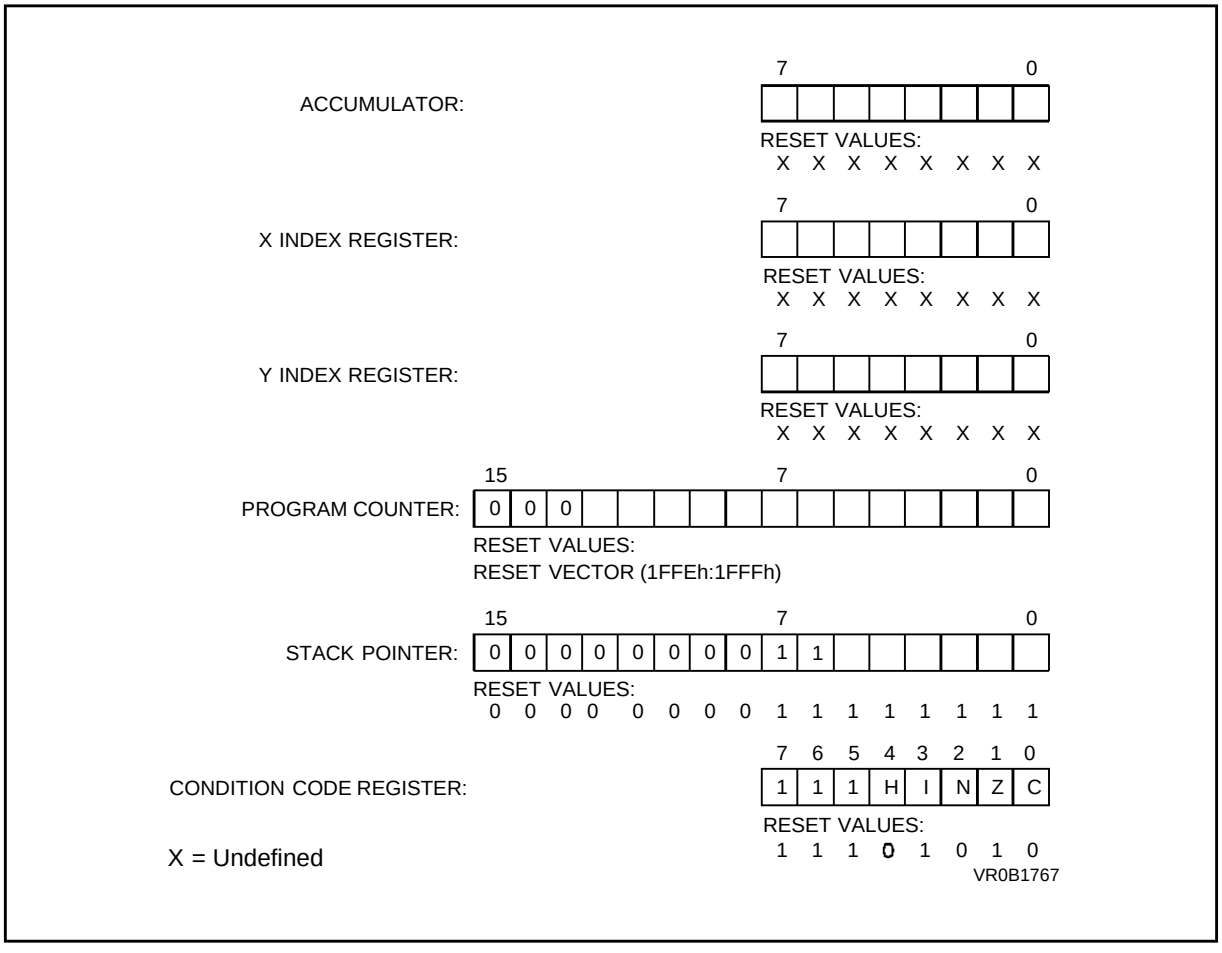
The 6 CPU registers are shown in the programming model in Figure 4. Following an interrupt, the registers are pushed onto the stack in the order shown in Figure 5. They are popped from stack in the reverse order. The Y register is not affected by these automatic procedures. The interrupt routine must therefore handle it, if needed, through the POP and PUSH instructions.

Accumulator (A). The accumulator is an 8-bit general purpose register used to hold operands and the results of the arithmetic and logic calculations as well as data manipulations.

Index Registers (X and Y). These 8-bit registers are used to create effective addresses or as temporary storage area for data manipulations. The cross-assembler generates a PRECEDE instruction (PRE) to indicate that the following instruction refers to the Y register. The Y register is never automatically stacked. Interrupt routines must push or pop it by using the POP and PUSH instructions.

Program Counter (PC). The program counter is a 16-bit register containing the address of the next instruction to be executed by the CPU. In the ST7294, only the 13 low order bits are used, bits 13, 14 and 15 are forced to "0".

Figure 4. Organisation of Internal CPU Registers



CENTRAL PROCESSING UNIT (Continued)

Stack Pointer (SP). The stack pointer is a 16-bit register. The 6 least significant bits contain the address of the next free location of the Stack. The 10 most significant bits are forced as indicated in Figure 4. They are reserved for future extensions of the ST72 family.

The Stack is used to save the CPU context on subroutine calls or interrupts. The user can also directly use it by means of the PUSH and POP instructions.

After a MCU reset or after the Reset Stack Pointer instruction (RSP), the Stack Pointer is set to its upper value (0FFh). It is then decremented after data has been pushed onto the Stack and incremented after data is popped from the Stack. When the lower limit is exceeded, the Stack Pointer wraps around to the stack upper limit. The previously stored information is then over written and therefore lost.

A subroutine call occupies two locations and an interrupt five locations.

Condition Code Register (CC).

The Condition Code register is a 5 bit register which indicates the result of the instruction just executed, as well as the state of the processor. These bits can be individually tested by a program and specific action may be taken as a result of their state. The following paragraphs describe each bit.

Half carry bit (H). The H bit is set to 1 when a carry occurs between the bits 3 and 4 of the ALU during an ADD or ADC instruction. The H bit is useful in BCD arithmetic subroutines.

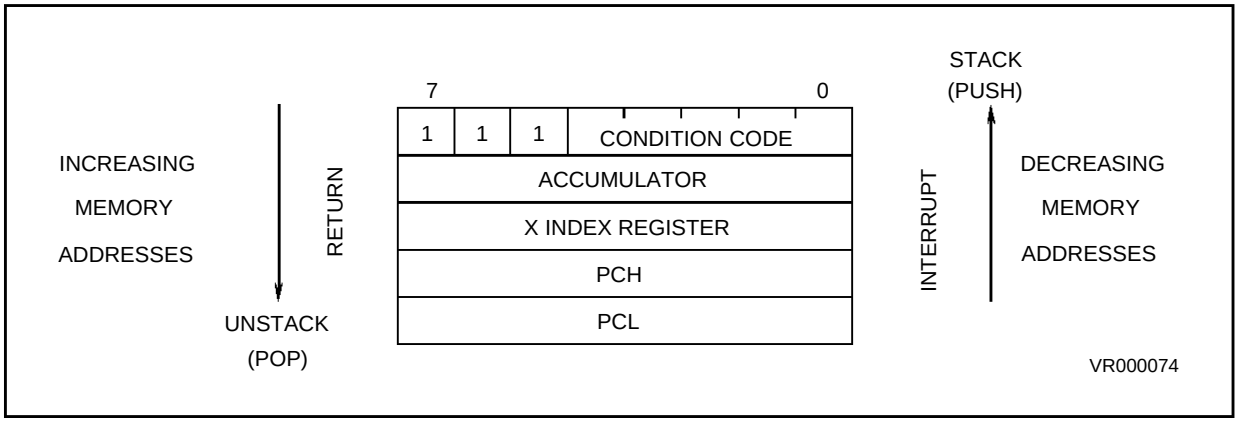
Interrupt mask (I). When the I bit is set to 1, all interrupts are disabled. Clearing this bit enables them. Interrupts requested while I is set are latched and can be processed when I is cleared (only one interrupt request per interrupt enable flag can be latched).

Negative (N). When set to 1, this bit indicates that the result of the last arithmetic, logical or data manipulation is negative (i.e. the most significant bit is a logic 1).

Zero (Z). When set to 1, this bit indicates that the result of the last arithmetic, logical or data manipulation is zero.

Carry/Borrow (C). When set, C indicates that a carry or borrow out of the ALU occurred during the last arithmetic operation. This bit is also affected during bit test, branch, shift, rotate and storage instructions.

Figure 5. Stacking Order



3 CLOCKS, RESET, INTERRUPTS & POWER SAVING MODES

3.1 CLOCK SYSTEM

3.1.1 General Description

The MCU accepts either a Crystal/Ceramic resonator or an external clock to provide the internal oscillator. The internal clock (CPU Clock) is derived by a divide-by-2 from the external oscillator frequency (f_{OSC}).

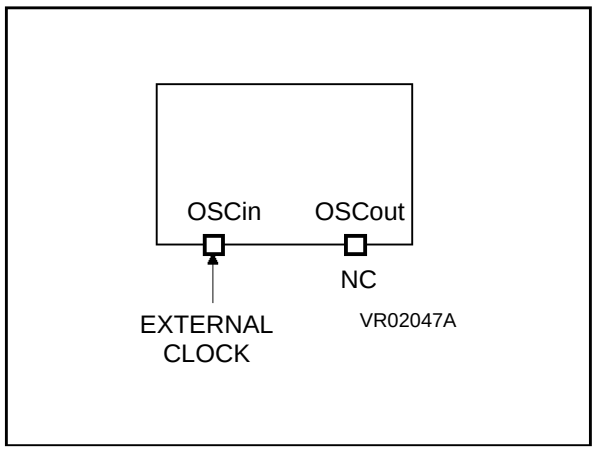
The slow mode function allows under software control to further slow down the internal clock, thus reducing power consumption. This feature is particular useful in WAIT mode.

The slow mode is entered by setting the SM bit in the Miscellaneous Register (0Ch). This mode affects all functions, including timer and EEPROM. The slow mode is exited by clearing SM or by entering the HALT mode.

3.1.2 Crystal

The internal oscillator is designed to interface with an AT-cut parallel resonant quartz crystal resonator in the frequency range specified for f_{osc}. The circuit shown on Figure 8 is recommended when using a crystal. The table lists the recommended capacitance and feedback resistance values.

Figure 6. External Clock Source Connections



Use of an external CMOS oscillator is recommended when crystals outside the specified ranges are to be used.

The crystal and components should be mounted as close as possible to the input pins to minimize output distortion and start-up stabilization time.

Figure 7. Equivalent Crystal Circuit

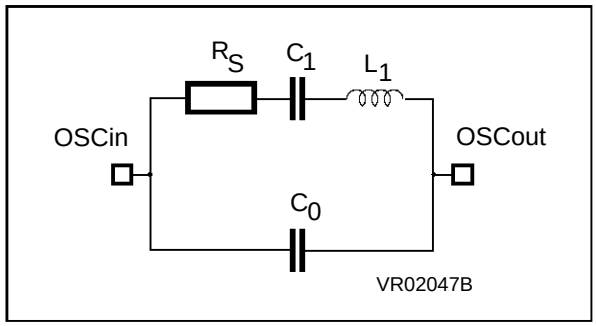
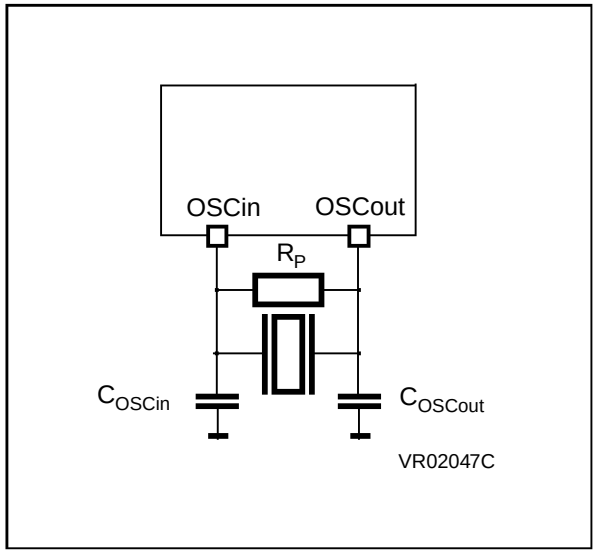


Figure 8. Crystal/Ceramic Resonator



CLOCK SYSTEM (Continued)

3.1.3 Ceramic Resonator

A ceramic resonator may be used in place of the crystal in low cost applications. The circuit on Figure 8 is recommended when using a ceramic resonator. The table lists the recommended capacitance and feedback resistance values. The manufacturer of the particular ceramic resonator being considered should be consulted for specific information.

3.1.4 External Clock

An external clock should be applied to the OSCin input with the OSCout pin not connected, as shown on Figure 6. The t_{OXOV} and t_{ILCH} specifications do not apply when using an external clock input. The equivalent specification of the external clock source should be used instead of t_{OXOV} or t_{ILCH}.

Table 2. Recommended Settings for Crystal

	2MHz	4MHz	Unit
R_{SMAX}	400	75	W
C_0	5	7	pF
C_1	8	12	nF
C_{OSCin}	15-40	15-30	pF
C_{OSCout}	15-30	15-25	pF
R_P	10	10	MΩ
Q	30	40	10^3

Table 3. Recommended Settings for Ceramic Resonator

	2-4MHz	Unit
R_{SMAX}	10	W
C_0	40	pF
C_1	4.3	nF
C_{OSCin}	30	pF
C_{OSCout}	30	pF
R_P	1-10	MΩ
Q	1250	

3.2 MISCELLANEOUS REGISTER

Miscellaneous Register (000Ch)

Register Address: 08h — Read/Write

Reset Value: 0001 000 (10h)

This is a miscellaneous 8-bit register, of which only 4 bits are used for interrupt, slow mode and Watchdog purposes.

7							0
-	INTP	INTN	-	-	-	SM	WDOG

b7, b4-b2 = Unused

b6 = **INTP**: *External Interrupt Positive* allows selection of the INT line triggering mode in conjunction with INTN. It can only be modified when the I bit of the CC Register is set.

b5 = **ININ**: *External Interrupt Negative* allows selection the INT line triggering mode in conjunction with INTP. It can only be modified when the I bit of the CC Register is set.

b1 = **SM**: *Slow Mode*. Setting this bit to 1 enables Slow Mode, thus reducing power consumption. In this mode, an extra divide-by-16 is added in the clock circuitry.

b0 = **WDOG**: *Watchdog System.* Whatever the WATCHDOG ENABLE MODE mask option, the watchdog counter is reset when WDOG is set to 1. When the MCU is configured with the “programmable enable” option, the WDOG bit is low following a reset. The bit must be set to enable the watchdog system. Only a reset can clear WDOG.

3.3 RESETS

3.3.1 Introduction

Resets are used to provide an orderly software start-up procedure or to exit the power-saving modes.

Two reset modes are provided: a Power-On Reset and an External Reset via the RESET pin.

A summary of the effects of both Reset modes on the different sections of the MCU is given in Table 4. For further information, please refer to the relevant section.

3.3.2 External Reset

The External Reset is an active-low input signal applied to the RESET pin of the MCU.

As shown in Figure 9, the RESET signal must stay low for a minimum of one and a half CPU clock cycles. A Reset causes the Reset Vector to be fetched at addresses 01FFEh and 01FFFh in order to be loaded into the PC.

The External Reset is used by the Watchdog system to reset the MCU. When active, the Power-On Reset circuitry pulls down the RESET pin. In both cases, the RESET pin may be used as an output to reset other devices. However, the pull down circuitry features current limiting to allow the connection of any input signal, including that originating from an RC type circuit.

An internal Schmitt trigger connected to the RESET pin improves noise immunity.

3.3.3 Power-On Reset (POR)

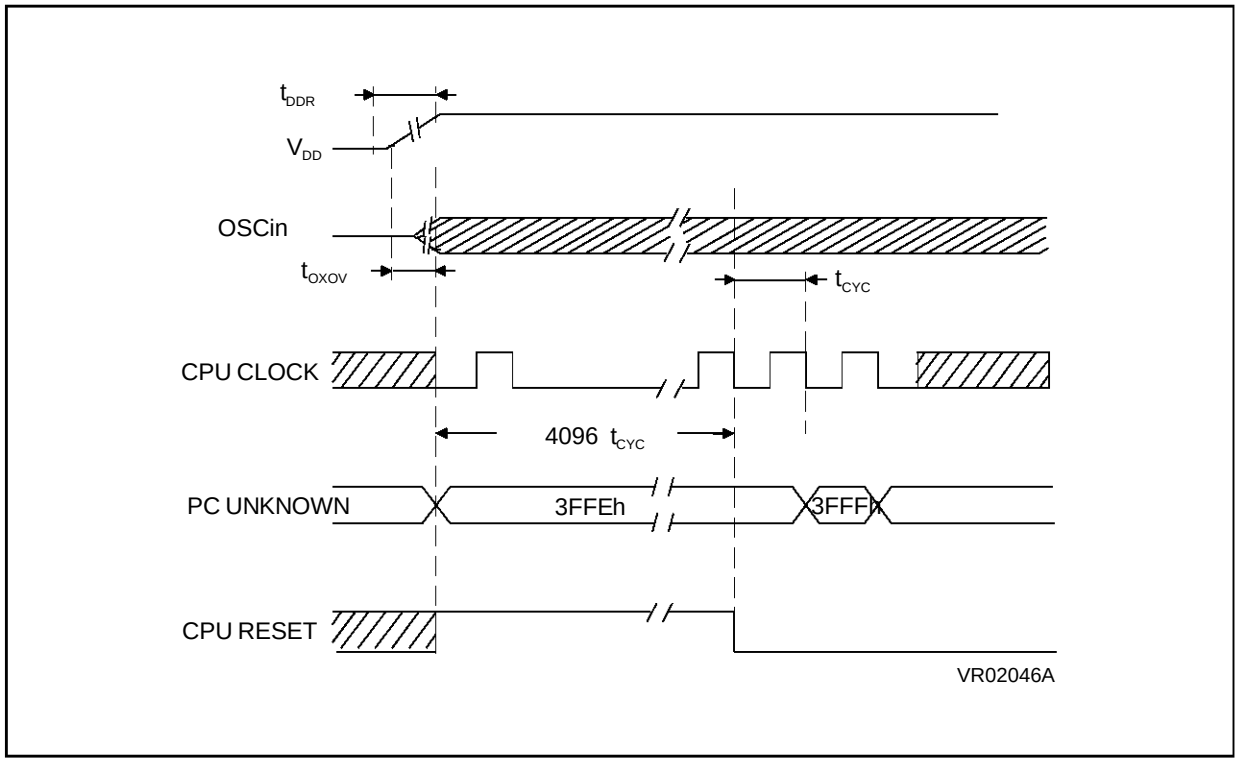
The Power-On Reset (POR) is generated on detection of a positive transition on V_{DD} (refer to Figure 9). This causes the Reset Vector to be fetched from addresses 01FFEh and 01FFFh, and loaded into the PC.

Internal circuitry provides a 4096 CPU clock cycle delay from the moment the oscillator becomes active. At the end of the Power-On Reset, the MCU can be maintained in the reset condition by means of the External Reset. The RESET pin can therefore be used to ensure V_{DD} has risen to a point where the MCU can operate properly before running the MCU program.

During the POR phase, the RESET pin is pulled low, thus permitting the MCU to reset other devices.

The Power-On Reset is strictly used for power up conditions and should not be used to detect any drop in the power supply voltage. There is no provision for a power-down reset.

Figure 9. Power-On Reset Timing Diagram



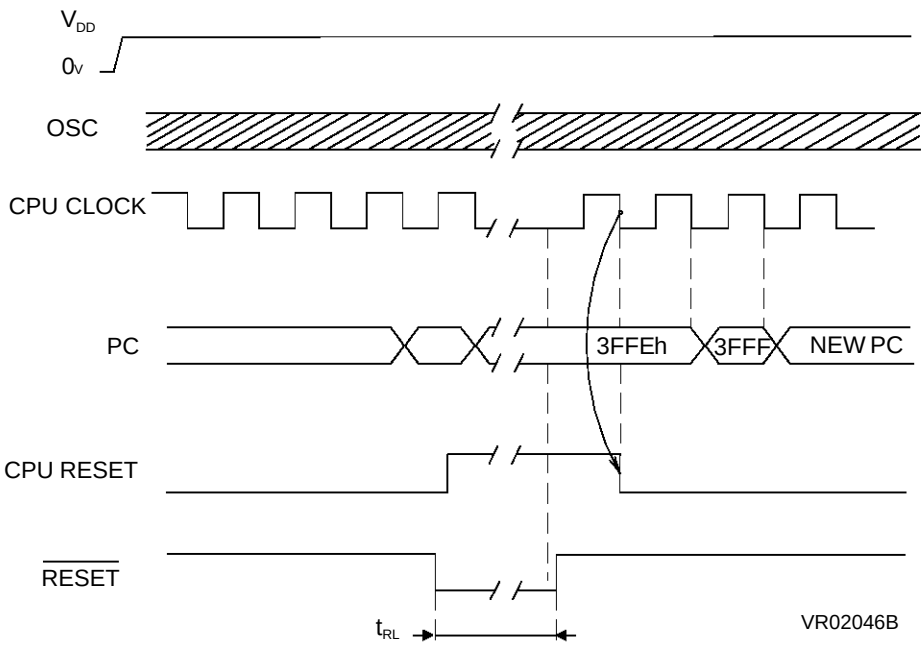
RESET (Continued)

Table 4. Actions caused by RESET, Power-on Reset (POR), WAIT and HALT

ACTION	RESET	POR	WAIT	HALT
Timer Prescaler reset to 0	X	X	-	-
Timer Counter set to FFFCh	X	X	-	-
All Timer enable bits reset to 0 (disabled)	X	X	-	-
Data Direction Registers reset to 0 (i.e. all I/O bits set as inputs)	X	X	-	-
Stack Pointer set to 00FFh	X	X	-	-
Internal Address Bus forced to Restart Vector	X	X	-	-
Interrupt Mask Bit (I-Bit, CCR) set to 1 (Interrupt disabled)	X	X	-	-
Interrupt Mask Bit (I-Bit, CCR) reset to 0 (Interrupt enabled)	-	-	X	X
HALT Latch reset	X	X	-	-
INT Latch reset	X	X	-	-
WAIT Latch reset	X	X	-	-
CPU Clock disabled (for 4096 clock cycles)	-	X	-	X
CPU Clock disabled(1)	-	X	X	X
Timer Clock disabled(1)	-	X	-	X
SM bit cleared	X	X	-	X
Watchdog Counter Rest	X	X	-	X
Watchdog WDOG bit reset	X	X	-	X
EEPROM control bits reset	X	X	-	-

Note 1: As can be seen in Table 4 above, WAIT mode only disables the CPU clock and not the Timer clock.

Figure 10. External Reset Timing Diagram



3.4 INTERRUPTS

3.4.1 Introduction

The ST7294 may be interrupted by one of four different methods: the three maskable hardware interrupts (INT, PORT C or TIMER) and the non-maskable software interrupt (TRAP). The Interrupt processing flowchart is shown in Figure 11. The maskable interrupts must be enabled in order to be serviced. However, disabled interrupts can be latched and processed when they are enabled. When an interrupt has to be serviced, the PC, X, A and CC registers are saved into the stack and the interrupt mask (I bit of the Condition Code Register) is set to prevent additional interrupts. The Y register is not automatically saved. The stack order is shown on Figure 5.

The PC is then loaded with the interrupt vector of the interrupt to service and the interrupt service routine runs (refer to Table 6 for vector addresses). It should finish by the IRET instruction which causes the contents of the registers to be recovered from the stack and normal processing to resume. Note that the I bit is then cleared if and only if the corresponding bit stored in the stack is zero.

Though many interrupts can be simultaneously pending, a priority order is defined. The RESET pin has the highest priority. Then, if the I bit is low, the decreasing priority order is TRAP, INT, timer input capture, timer output compare, timer overflow and PORT C. If the I bit is set, TRAP is the only enabled interrupt.

Interrupts allow the processor to leave low power modes. Refer to LOW POWER MODES for further information.

3.4.2 Software Interrupt

The software interrupt is the TRAP executable instruction. The interrupt is recognized when the TRAP instruction is executed, regardless to the I bit state. When the interrupt is recognized, it is serviced according to the flowchart on Figure 10.

3.4.3 External Interrupt

The external interrupt is generated through the INT pin. The interrupt is enabled if the I bit of the CCR is cleared.

The INTN and INTP bits of the Miscellaneous Register (0Ch) allow selection of the interrupt triggering mode among the 4 available ones. Refer to Table 5 for the triggering mode coding.

In order to avoid conflicts and spurious interrupts, the external interrupt options can only be changed when the I bit is set. Any attempt to change the options while I is reset fails. When the options are changed any pending interrupt is lost.

When an enabled interrupt occurs, normal processing is suspended at the end of the current instruction execution. It is then processed according to the flowchart on Figure 11.

If the interrupt is disabled (I high), the triggering edge of the INT line is internally latched and the interrupt remains pending to be processed as soon as the interrupt is enabled (the low level sensitive interrupt is not latched and can therefore not remain pending). This internal latch is cleared in the first part of the service routine. Therefore, one, and one only, external interrupt can be latched and serviced as soon as enabled.

Figure 12 shows the mode timing diagram for the interrupt line. Two methods are described. The first method shows single pulses on the interrupt line spaced far enough apart to be serviced. The minimum time between pulses is a function of the number of cycles required to execute the interrupt service routine plus 21 cycles. Once a pulse occurs, the next pulse should not occur until the MCU software has exited the routine (an IRET instruction occurs).

The second configuration shows several interrupt lines “wire-ORed” to form the interrupts at the processor. Thus, if after servicing one interrupt the interrupt line remains low, then the next interrupt is recognized.

Application Note ($\overline{\text{INT}}$ pin operation): The $\overline{\text{INT}}$ pin is used as an external interrupt input signal, and also to select a non-user autotest mode reserved exclusively for internal use by SGS-THOMSON Microelectronics. There is no pull-up resistor connected internally to the INT pin. Thus, in order to avoid unexpected entry in non-user mode, the INT pin must be tied to V_{DD} if not used, or connected to V_{DD} through a diode if used as an input. See Caution message in section Section 1.2 PIN DESCRIPTION.

INTERRUPTS (Continued)

3.4.4 PORTC Interrupt

The PORTC Interrupt can be generated on the falling edge of one of pins PC0-PC5, if it is defined as an interrupt source. When an enabled interrupt occurs, normal processing is suspended at the end of the current instruction execution. It is then processed according to the flowchart on Figure 11.

If the interrupt is disabled (I high), the triggering edge of the wake-up interrupt is internally latched and the interrupt remains pending, to be processed as soon as the interrupt is enabled. This internal latch is cleared in the first part of the service routine. Therefore one, and only one, external interrupt can be latched and serviced at any instant.

3.4.5 Timer Interrupt

Two different timer interrupt flags are capable of causing a timer interrupt when they are active, if both the I bit of the CCR is reset, and if the corresponding enable bit is set. If either of these conditions is false, the interrupt is latched and thus remains pending.

The interrupt flags are located in the Timer Status Register (0013h). The Enable bit are in the Timer Control Register (0012h).

When an enabled interrupt occurs, normal processing is suspended at the end of the current instruction execution. It is then serviced according to the flowchart on Figure 11. Software in the Timer Service Routine must determine the priority and cause of the timer interrupt by examining the interrupt flags and the status bits located in the TSR.

The general sequence for clearing an interrupt is an access to the status register while the flag is set followed by a read or write of an associated register. Note that the clearing sequence resets the internal latch. A pending interrupt (i.e. waiting for being enabled) will therefore be lost if the clear sequence is executed.

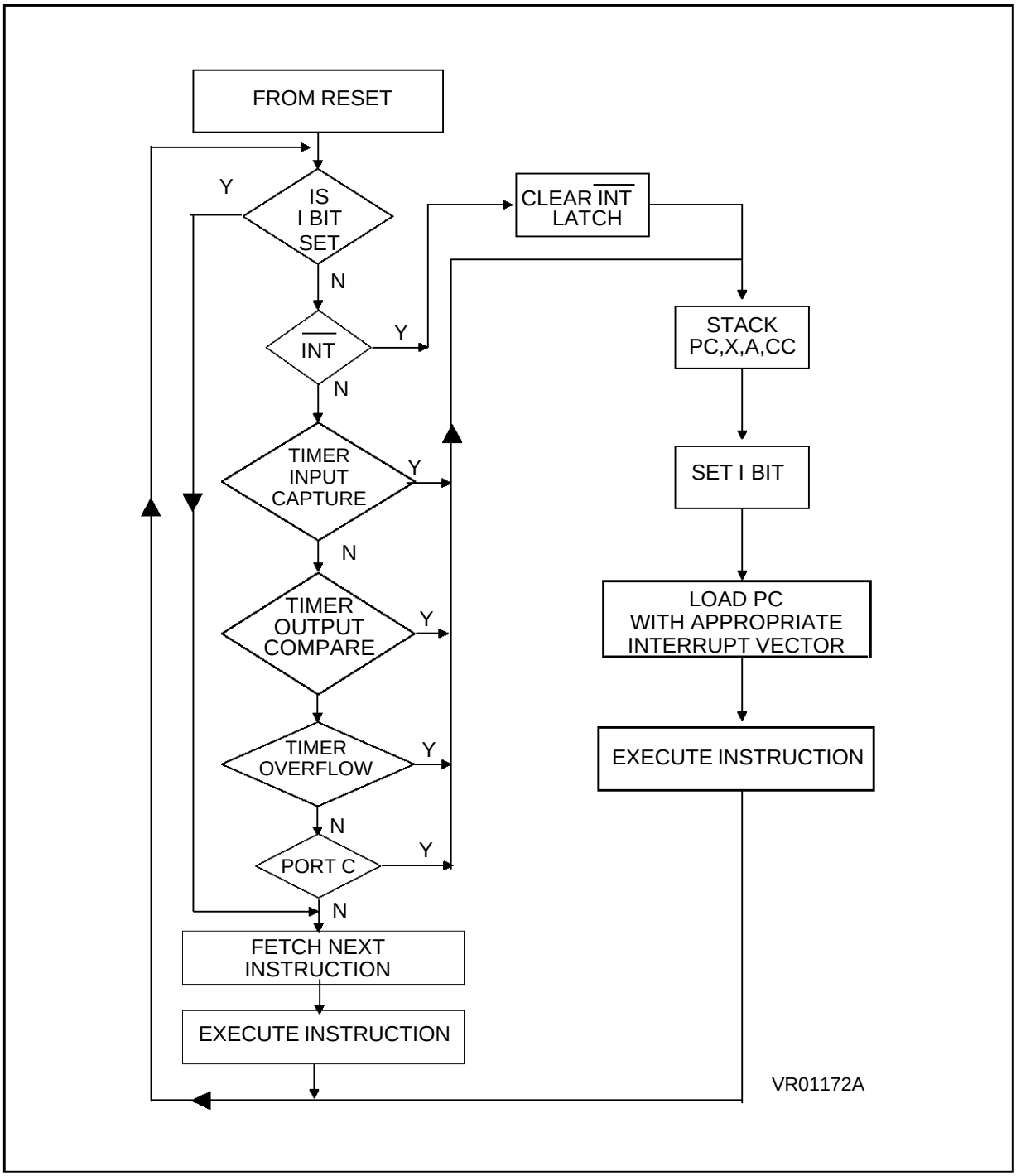
Refer to Section 4.3 16-BIT TIMER, for further information.

Table 5. External Interrupt Options

INTP	INTN	External Interrupt Options
0	0	Negative edge and low-level sensitive
0	1	Negative edge sensitive only
1	0	Positive edge sensitive only
1	1	Positive and negative edge sensitive

INTERRUPTS (Continued)

Figure 11. Interrupt Processing Flow Chart

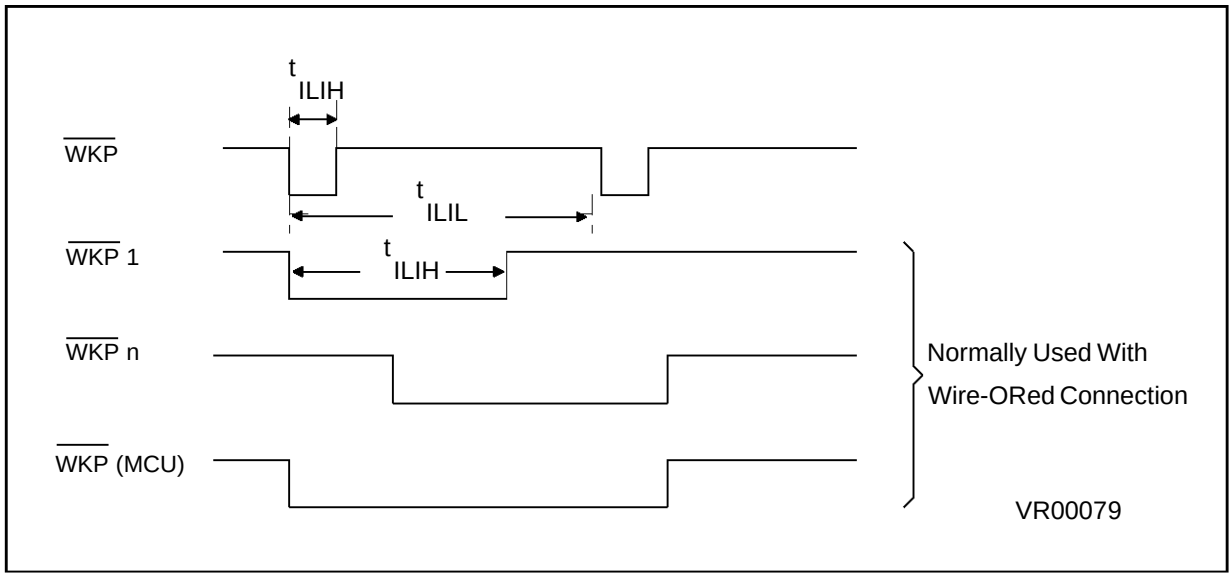


INTERRUPTS (Continued)

Table 6. Interrupt and Reset Priorities

Vector Address	Interrupt Source	Masked by	Priority
			Highest
1FFEh,1FFFh	RESET and POWER-ON (POR)	none	
1FFCh,1FFDh	SOFTWARE Interrupt (TRAP)	none	
1FFAh,1FFBh	EXTERNAL Interrupt (INT)	I-Bit	
1FF8h,1FF9h	TIMER INPUT Capture	I-Bit	
1FF6h,1FF7h	TIMER OUTPUT Compares (1 and 2)	I-Bit	
1FF4h,1FF5h	TIMER OVERFLOW	I-Bit	
1FF2h,1FF3h	Reserved	I-Bit	
1FF0h,1FF1h	PORT C Wake-up	I-Bit	
			Lowest

Figure 12. Timing Diagram for the Interrupt Line



3.5 WATCHDOG SYSTEM

The Watchdog System consists in a divide-by-8 counter and a fixed divide-by-1024 prescaler. It is controlled through bit WDOG of the Miscellaneous Register. Two mask options are provided.

The Watchdog Enable mode mask option selects the state of the Watchdog System after an external or a power-on reset. In the “programmable enable” option, a reset causes the watchdog to be disabled and the counter to be forced to zero. When the watchdog is configured with the “programmable enable” option, the watchdog system is enabled by setting the WDOG bit of the Miscellaneous Register (0Ch). Only an external or a power-on reset can clear WDOG and disable the watchdog system.

Whatever the option, when the watchdog counter is enabled, it is driven by the CPU clock through the divide-by-1024 prescaler (i.e. the counter clock period is 1024 CPU clock cycles). It is reset to zero by writing WDOG at 1. A system reset is generated if the counter reaches it maximum count (8). To avoid a system reset, the software must therefore reset the counter at least after a timer t_{DOG} from the last clear or from the time the watchdog system has been enabled.

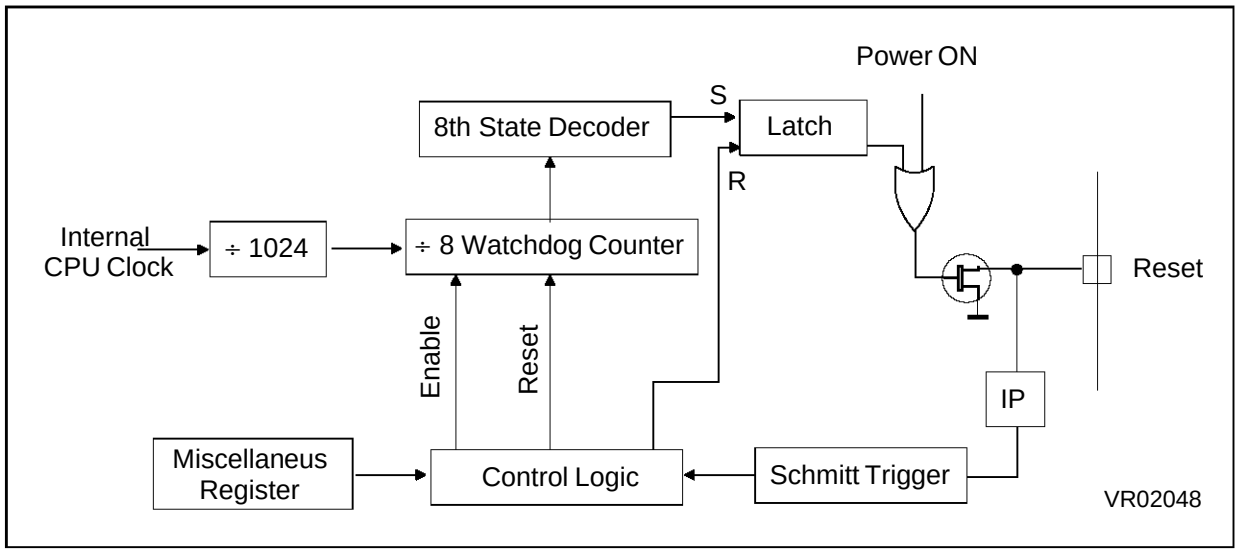
Care has to be taken when enabling the counter (“programmable enable” option only). The prescaler is actually in an unknown state at the time WDOG is set. The first rising edge can thus be sent to the watchdog counter after a time comprised between 0 and 1024 CPU clock cycles. In this mode, the first reset of the watchdog counter should therefore not occur later than 6x1024 CPU clock cycles after it has been enabled.

The system reset is generated by pulling down the RESET pin for at least one and a half CPU clock cycle. The state of the RESET pin is re-entered, thus causing an external reset to be issued.

The WATCHDOG DURING WAIT mask option allows to determine the watchdog function during the WAIT low power mode. In the “active during WAIT” option, the watchdog is kept active, thus able to reset the MCU if it remains in WAIT mode longer than the watchdog timeout period. In the “suspended during WAIT” option, it suspends operation during the WAIT mode and resets its counter. It will then resume operation when exiting the WAIT mode.

The HALT mode is inhibited when the watchdog system is enabled. However if a HALT instruction is executed while it is enabled, a watchdog reset is immediately generated.

Figure 13. Watchdog Block Diagram



3.6 POWER SAVING MODES

Table 4 gives a list of the different sections affected by the Power Saving modes. For detailed information on specific devices, please refer to the appropriate sections.

Figure 14. HALT Function Flow Chart

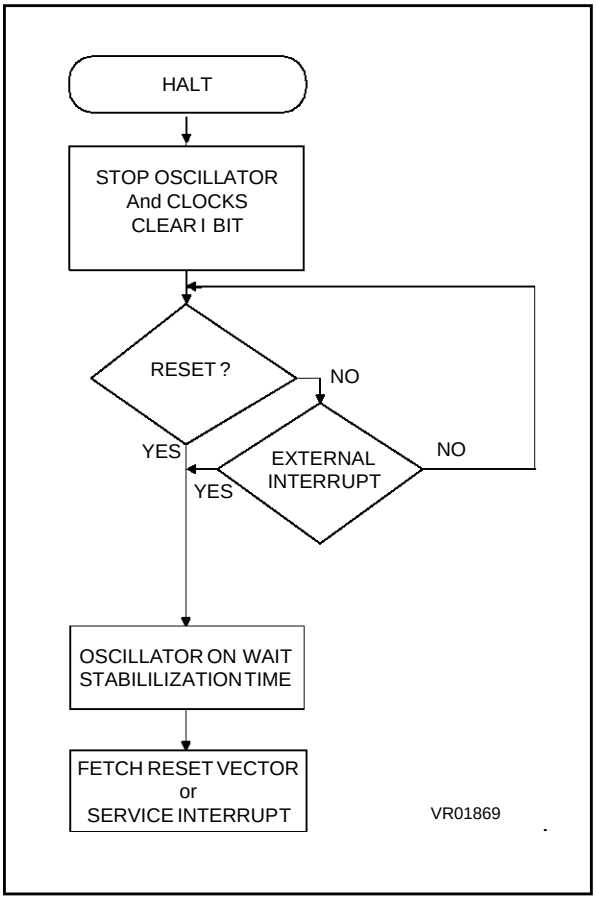
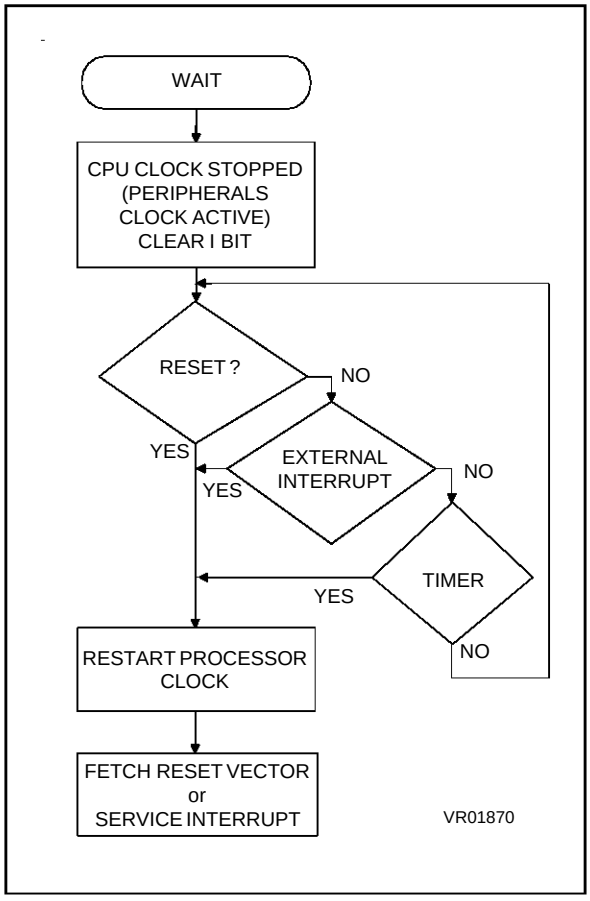


Figure 15. WAIT Flow Chart



LOW POWER MODES (Continued)

3.6.1 HALT Mode

The HALT Power Saving mode is the lowest power consumption mode. The HALT mode is entered by executing the HALT instruction. The internal oscillator is then turned off, causing all internal processing to be stopped, including the operation of the on-chip peripherals.

When entering the HALT mode, the I bit in the Condition Code Register is cleared. Interrupts are thus enabled and, on receiving an interrupt, the MCU will be restarted and will run at its nominal speed (see Section 3.1 CLOCK SYSTEM). All other registers and memory remain unaltered and all I/O lines remain unchanged.

The MCU can exit the HALT mode upon reception of either an external interrupt, a PORT B derived interrupt, or a power-on or external reset. The oscillator is then enabled and a stabilization delay is initiated before enabling CPU operation. The stabilization time period is equivalent to 4096 CPU clock cycles.

After the start-up delay, the CPU then proceeds to service the interrupt which has woken it up by fetching the relevant Interrupt Vector.

3.6.2 WAIT Mode

This mode is a Power Saving mode, but the power consumption is higher than in the HALT mode.

The WFI instruction places the MCU in the WAIT mode; in this mode, the internal clock remains active but all CPU processing is stopped.

While in the WAIT mode, the I bit in the Condition Code register is cleared in order to enable all interrupts. All other registers and memory remain unaltered and all parallel I/O lines remain unchanged.

An interrupt or a reset causes the MCU to exit the WAIT mode. An interrupt while the MCU is in this mode causes the corresponding interrupt vector to be fetched, the interrupt routine to be executed and normal processing to resume. A reset causes the program counter to fetch the reset vector and processing starts as for a normal reset.

3.6.3 DATA RETENTION Mode

The RAM contents and the CPU registers are retained even with supply voltages as low as 2.0V. This is referred to as the Data Retention mode. In this mode Data is protected but the device is not guaranteed to operate.

4 ON-CHIP PERIPHERALS

4.1 EEPROM

4.1.1 Introduction

The ST7294 MCU includes a 256 byte EEPROM memory for temporary data storage.

4.1.2 Functional Description

An internal charge pump avoids the need for an external high voltage supply for the EEPROM erasure and programming functions.

8 data registers allow simultaneous write or erase of 1 to 8 bytes in the EEPROM array.

As shown on Figure 16, the EEPROM is organised as an array composed of 8 columns by 32 rows. Rows are selected by bits A7, A6, A5, A4, A3, while columns are associated with the bits in an 8-bit data register.

4.1.3 Read Operation (E2LAT=0).

The EEPROM can be read just as a normal ROM when the E2LAT bit of the Control Register is low. When E2LAT is low, the E2PGM and E2ERA bits are also forced low.

4.1.4 Erase/Write Operation (E2LAT=1)

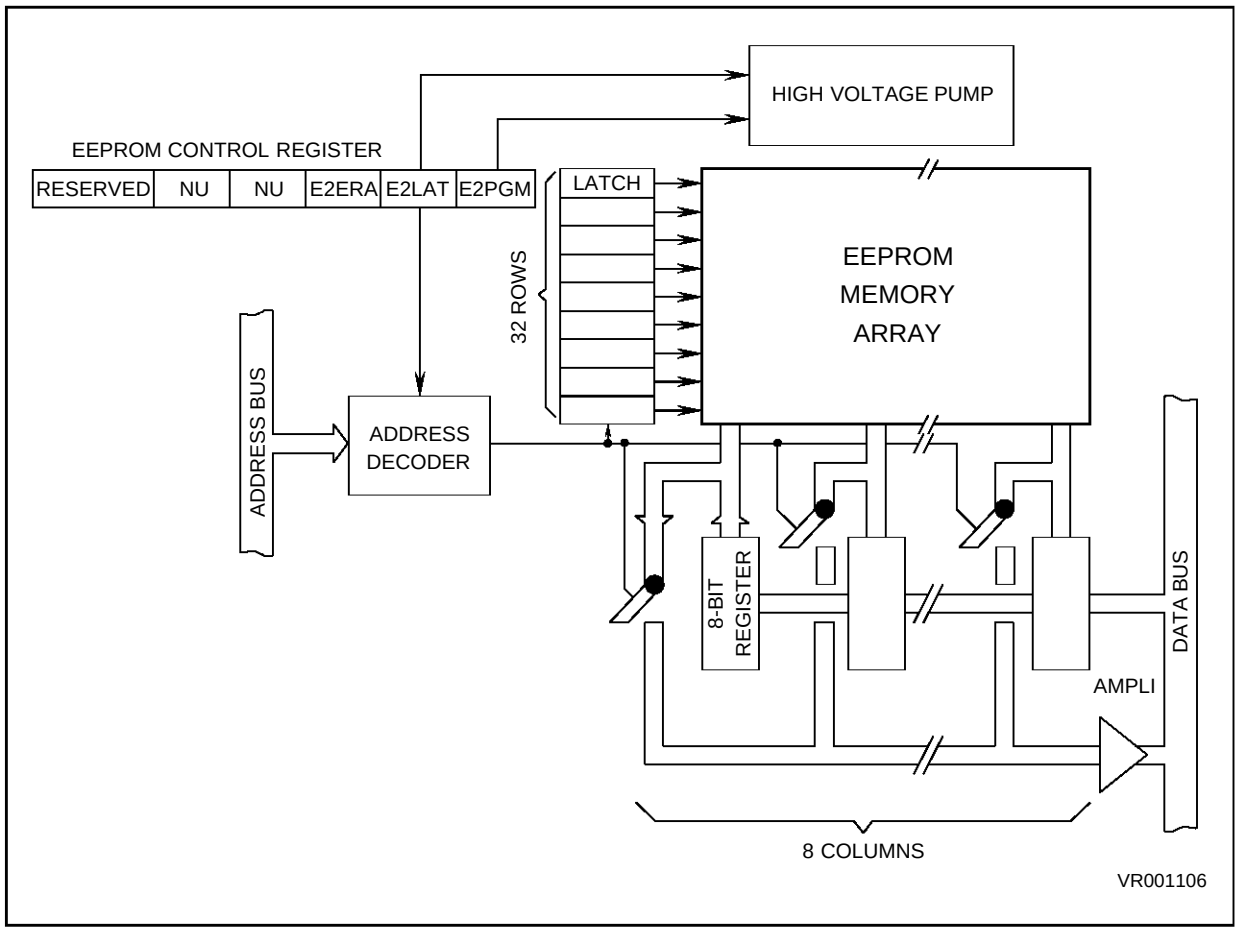
When E2LAT is set to 1, a write to an EEPROM location latches the data in the 8-bit register corresponding to the decoded column and marks the decoded row.

As there are 8 columns in each row, up to 8 locations (having the same A7, A6, A5, A4, A3 address bits) may be written or erased simultaneously.

To **erase** bytes: set the E2LAT and E2ERA bits, write to the EEPROM addresses to be erased (data value is not significant), and then set the E2PGM bit to turn the charge pump on.

To **write** bytes: set the E2LAT bit, write the data in the appropriate EEPROM addresses, and then set the E2PGM bit to turn the charge pump on.

Figure 16. EEPROM Block Diagram



EEPROM (Continued)

Note 1. Bytes must always be erased prior to being written.

Note 2. E2LAT must be kept high during a time period designated as t_{PROG} and then be cleared.

Note 3. When E2LAT is high, access to the EEPROM array is impossible.

Note 4. It is impossible to perform successive write or erase cycles without clearing E2LAT.

Note 5. The device is delivered with the EEPROM memory filled with the value FFh.

Warning: *User programs must not run from the EEPROM (reserved for data only).*

4.1.5 EEPROM Control Register

Register Address: 07h — Read/Write

Reset Value: 0000 0000<N> (00h)

7							0
Res	Res	Res	-	-	E2ERA	E2LAT	E2PGM

This register contains the bits required to read, erase and program the EEPROM. They are defined as follows:

Bits 7, 6, 5 = Reserved

Bits 4,3 = Unused

Bit 2 = **E2ERA** *EEPROM Erase*

E2ERA must be set to 1 for an erase operation. It must be set after or at the same time as E2LAT. It cannot be changed once 1 EEPROM address is selected. It is held low when E2LAT is low. It is therefore automatically reset when E2LAT is reset.

Bit 1 = **E2LAT** *EEPROM Latch Enable*

When E2LAT is reset to 0, data can be read from the EEPROM. When it is set to 1 and E2PGM reset to 0, a write into the EEPROM array causes the data to be latched, according to the address into one of 8 data registers. An additional bit is latched to select the row. The selected columns and row determine the locations involved in the next erase or programming operation. E2LAT must be cleared after each programming or erase operation. E2ERA and E2PGM are forced low when E2LAT is low.

Bit 0 = **E2PGM** *EEPROM Program Mode*

This bit allows to switch on or off the internal charge pump. When set to 1, the charge pump generator is on: the high voltage is applied to the EEPROM array. When low, the charge pump generator is off. E2PGM can only be reset by resetting E2LAT.

4.2 I/O PORTS

4.2.1 Functional Description

Ports A and B are 8-bit I/O ports, port C is a 6-bit I/O port. Each of their pins may be individually configured under software control as either input or output.

Each bit of any Data Direction Register corresponds to an I/O pin on the associated port. A bit must be set to configure its associated pin as output and must be cleared to configure its associated pin as input. The Data Direction Registers can be written or read.

The typical I/O circuit is shown on Figure 17. Any write to an I/O port updates the port output register even if it is configured as input. Any read of an I/O port returns either the data latched in the port output register (output configured pins) or the value at the I/O pin (input configured pins) (see Table 7).

At power-on or external reset, all DDR's are cleared, which configures all port A, B and C pins as inputs, but the port output registers are not initialized. Thus, the I/O port should be written before setting the DDR bits to avoid undefined levels.

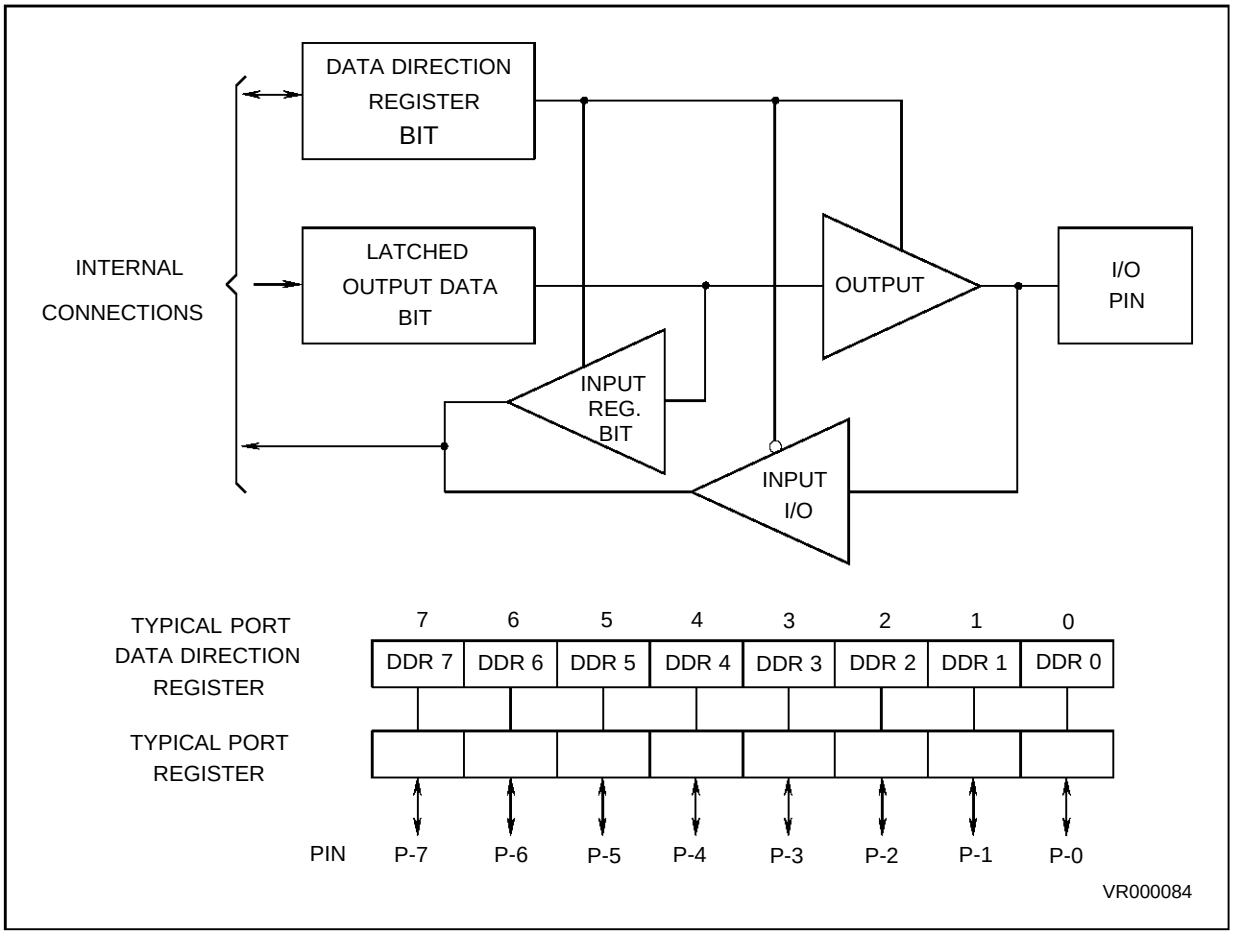
Depending on the chosen mask option, Port A bits can be defined as an Input/Output line or as an Input/Output drain line. When programmed as input, each port line may be tied to V_{DD} through an internal pull-up resistor (by option).

Depending on the chosen mask option, PORT B bits can be tied to V_{DD} through an internal pull-up resistor if defined as input.

Depending on the chosen mask option, PORT C bits can be configured as wake-up interrupt input with an internal pull-up resistor. To enter this mode, the corresponding bit in DDR must be set to 1 and the corresponding bit in DR must be set to 0.This mode can only be reached for PC0 and PC1 if they have not been configured as ICAP or OCMP1 respectively.

All unused I/O lines should be tied to an appropriate logic level (either V_{DD} or V_{SS}).

Figure 17. Typical I/O pin configuration of Ports A and C



I/O PORTS (Continued)

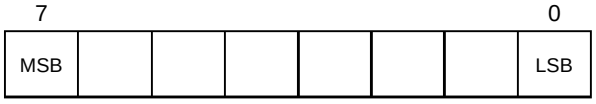
Table 7. I/O Pin Logic

R/$\overline{W}$*	DDR	I/O Pin Functions
0	0	The I/O pin is in input mode. Data is written into the output data latch.
0	1	Data is written into the output data latch and output the I/O pin.
1	0	The state of the I/O pin is read.
1	1	The I/O pin is in an output mode. The output data latch is read.

Note (*): $\overline{RW}$ is an internal signal.

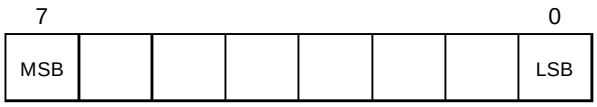
DATA REGISTERS

Port A: 00h
Port B: 01h
Port C: 02h
Read/Write
Reset Value: Undefined



DATA DIRECTION REGISTERS

Port A: 04h
Port B: 05h
Port C: 06h
Read/Write
Reset Value: 00h (as inputs)



4.3 16-BIT TIMER

4.3.1 Introduction

The 16-bit programmable timer consists of a 16-bit free running counter driven by a mask option configurable prescaler and control logic for one input capture and two output compare registers. It can be used for many purposes including pulse length measurement of one input signal and generation of one output waveform.

Because the timer has a 16-bit architecture, each of its specific function block is represented by two registers. These registers contain the high order byte and low order byte of that function. However an access to the high order byte inhibits that specific timer capability until the low order byte is also accessed.

Note that correct software procedures should set the I bit of the Condition Code Register before accessing the high order byte to prevent an interrupt from occurring between the accesses to the high and low order bytes of any register.

The timer block diagram is shown on Figure 18.

4.3.2 Functional Description

4.3.2.1 Counter

The key element of the programmable timer is a 16-bit free running counter or counter register. It is preceded by a prescaler which divides the internal clock by four. This counter is incrementing by each event.

Software can read the counter at any time without affecting its value. It can be read from two locations, the Counter Register (0018h, 0019h) and Alternate Counter Register (001Ah, 001Bh). The only difference between these two read-only registers is the way the overflow flag TOF is handled during a read sequence.

A read sequence containing only a read of the least significant byte of the free running counter (from either the Counter Register or the Alternate Counter Register) will receive the LSB of the count value at the time of the read. A read of the most significant byte (from either the Counter Register or the Alternate Counter Register) simultaneously returns the MSB of the count value and causes the LSB to be transferred into a buffer.

The buffered value remains unchanged until the 16-bit read sequence is completed, even if the user reads the MSB several times. The read sequence is completed by reading the free running counter LSB, which actually returns the buffered value.

As shown on Figure 20 and Figure 21, the free running counter is configured to FFFCh during reset. During a Power-On Reset (POR), the counter is also configured to FFFCh and begins running after the oscillator start-up delay.

When the counter rolls over from FFFFh to 0000h, the Timer Overflow flag (TOF) of the Timer Status Register (TSR) is set. A timer interrupt is then generated if the TOIE enable bit of the Timer Control Register (TCR) is set, provided the I bit of the CCR is cleared. If one of these conditions is false, the interrupt remains pending to be issued as soon as they are both true. The Interrupt Request is cleared by reading TSR, while TOF is set followed by an access (read or write) to the LSB of the Counter Register.

The TOF flag is not affected by accesses to the Alternate Counter Register. This feature allows simultaneous use of the overflow function and reads of the free running counter at random times (for example, to measure on elapsed time) without risking to clear the TOF flag erroneously. Accesses to the Timer without the intention of servicing the TOF flag should therefore be performed to the Alternate Counter Register while only the TOF service routine accesses the Counter Register.

The free running counter can be reset under software control. This is performed by writing to the LSB of either the Counter Register or the Alternate Counter Register. The counter and the prescaler are then configured to their reset conditions. This reset also completes any 16-bit access sequence. All flags and enable bits are unchanged.

The value in the counter registers repeats every 262,144 internal processor clock cycles. As shown on Figure 20, the counter increment is triggered by a falling edge of the CPU clock.

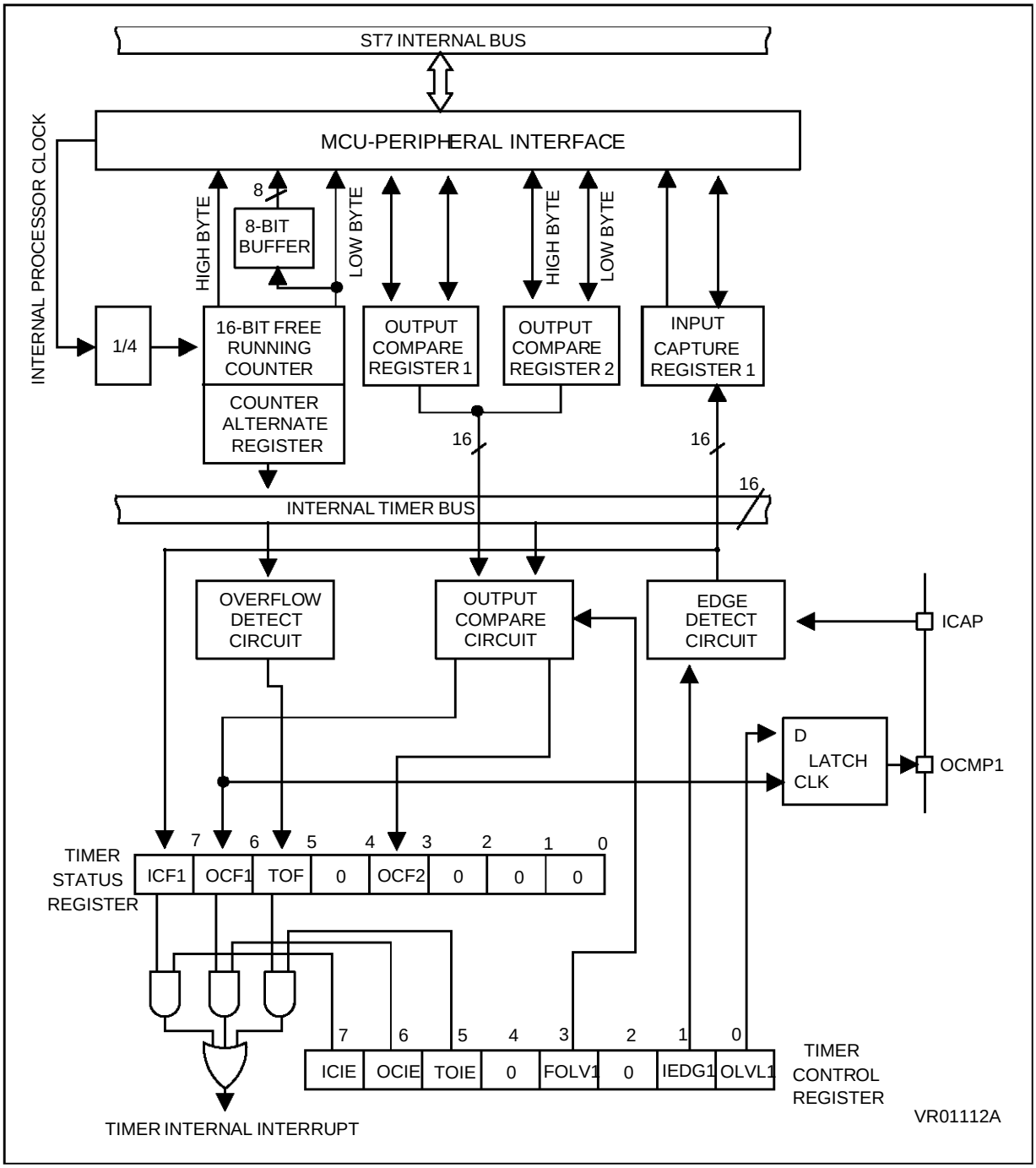
The timer is not affected by the WAIT mode. In the HALT mode, the counter stops counting until the mode is exited. Counting then resumes from previous count (MCU awoken by an interrupt) or from reset count (MCU awoken by a reset).

4.3.2.2 Input Capture

The ST7294 features an Input Capture register and an Input Capture interrupt enable bit. The 16-bit Input Capture Register, ICR1, is made up of two 8-bit registers: the most significant byte register, ICHR1, located at 014h, and the least significant byte register (ICLR1) located at 015h. The read-only register ICR1 is used to latch the value of the free running counter after a defined transition is sensed by the input capture edge detector on ICAP. This transition is software programmable through the IEDG1 bit of the Timer Control Register. When IEDG1 is set, a rising edge triggers the capture; when IEDG1 is low, the capture is triggered by a falling edge.

16 BIT TIMER (Continued)

Figure 18. Timer Block Diagram



16-BIT TIMER (Continued)

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When an input capture occurs, flag ICF1 in the Timer Status Register (TSR) is set. An interrupt is requested if the interrupt enable bit ICIE of the TCR is set, provided the I bit of the CCR is cleared. Otherwise, the interrupt remains pending until both conditions become true. The condition is cleared by reading the TSR followed by an access (read or write) to the LSB of ICR1.

The result stored in ICR1 is one more than the value of the free running counter on the rising edge of the internal processor clock preceding the active transition at pin ICAP (see Figure 19). This delay is required for internal synchronization. Therefore, the timing resolution of the input capture system is 1/4 internal clock cycle.

The free running counter is transferred to ICR1 on each proper signal transition regardless of whether the Input Capture Flag ICF1 is set or cleared. The ICR1 always contains the free running counter value which corresponds to the most recent input capture.

After a read of the MSB of ICR1 (ICHR1), counter transfer of input capture is inhibited until the LSB of ICR1 (ICLR1) is also read. This characteristic forces the minimum pulse period attainable to be determined by the time to service the interrupt and to execute the interrupt routine.

A read of ICLR1 does not inhibit the counter transfer. Again, minimum pulse periods are the ones which allow software to read the least significant byte and perform needed operations. There is no conflict between the read of ICR1 and the running counter transfer since they occur on opposite edges of the internal processor clock (see Figure 19).

The ICR1 is undetermined at power-on and is not affected by an external reset. Hardware circuitry has to provide protection from generating a wrong input capture when changing the edge sensitivity option of ICAP pin through the IEDG1 bit.

During the HALT mode, if at least one valid input capture edge occurs at the ICAP pin, the input capture detect circuitry is armed. This action does not set any timer flags nor “wake-up” the MCU. If the MCU is awaken by an interrupt, there is an active input capture flag and data from the first valid edge that occurred during the HALT mode. If the HALT mode is exited by a reset, the input capture detect circuitry is reset and thus, any active edge that happened during the HALT mode is lost.

4.3.2.4 Output Compare

There are two output compare registers: Output Compare Register 1 and 2 (OCR1 and OCR2). They can be used for several purposes such as controlling an output waveform or indicating when a period of time has elapsed. OCMP1 pin is associated with output compare 1; no pin is associated with output compare 2.

The Output Compare Registers are unique because all bits are readable and writable and are not affected by the timer hardware and reset. If a compare function is not used, the two bytes of the corresponding Output Compare Registers can be used as storage locations.

Note that the same output compare interrupt enable bit is used for both output compares.

4.3.2.5 Output Compare Register 1

The Output Compare Register 1 (OCR1) is a 16-bit register, which is made up of two 8-bit registers: The most significant byte register (OCHR1) at address 0016h and the least significant byte register (OCLR1) at address 0017h. The content of OCR1 is compared with the content of the free running counter once during every timer clock cycles, i.e. once every 8, 4 or 2 internal processor clock periods according to the TIMER CLOCK mask option. If match is found, the Output Compare Flag OCF1 of the TSR is set and the Output Level bit (OLVL1) of the TCR is clocked to the OCMP1 pin (see output compare timing diagram on Figure 19 and Figure 21).

OLVL1 is copied to the corresponding output level latch and hence, to the OCMP1 pin regardless of whether the Output Compare Flag (OCF1) is set or not. The value in the OCR1 and the OLVL1 bit should be changed after each successful comparison in order to control an output waveform or establish a new elapsed timeout.

An interrupt accompanies a successful output compare if the corresponding interrupt enable bit OCIE of the TCR is set, provided the I-bit of the CCR is cleared. Otherwise, the interrupt remains pending until both conditions are true. It is cleared by a read of TSR followed by an access to the LSB of the OCR1.

16-BIT TIMER (Continued)

After a processor write cycle to the OCHR1 register, the output compare function is inhibited until the OCLR1 is also written. Thus, the user must write both bytes if the MSB is written first. A write made to only the LSB will not inhibit the compare function. The minimum time between two successive edges on the OCMP1 pin is a function of the software program.

The OCMP1 output latch is forced low during reset and stays low until valid compares change it to a high level. Because the OCF1 flag and the OCR1 are indeterminate at power-on and are not affected by an external reset, care must be exercise when initiating the output compare function with software. The following procedure is recommended to prevent the OCF1 flag from being set between the time it is read and the write to OCR1:

Write to OCHR1 (further compares are inhibited).

Read the TSR (first step of the clearance of OCF1 [it may be already set]).

Write to OCLR1 (enables the output compare function and clears OCF1).

4.3.2.6 Output Compare Register 2

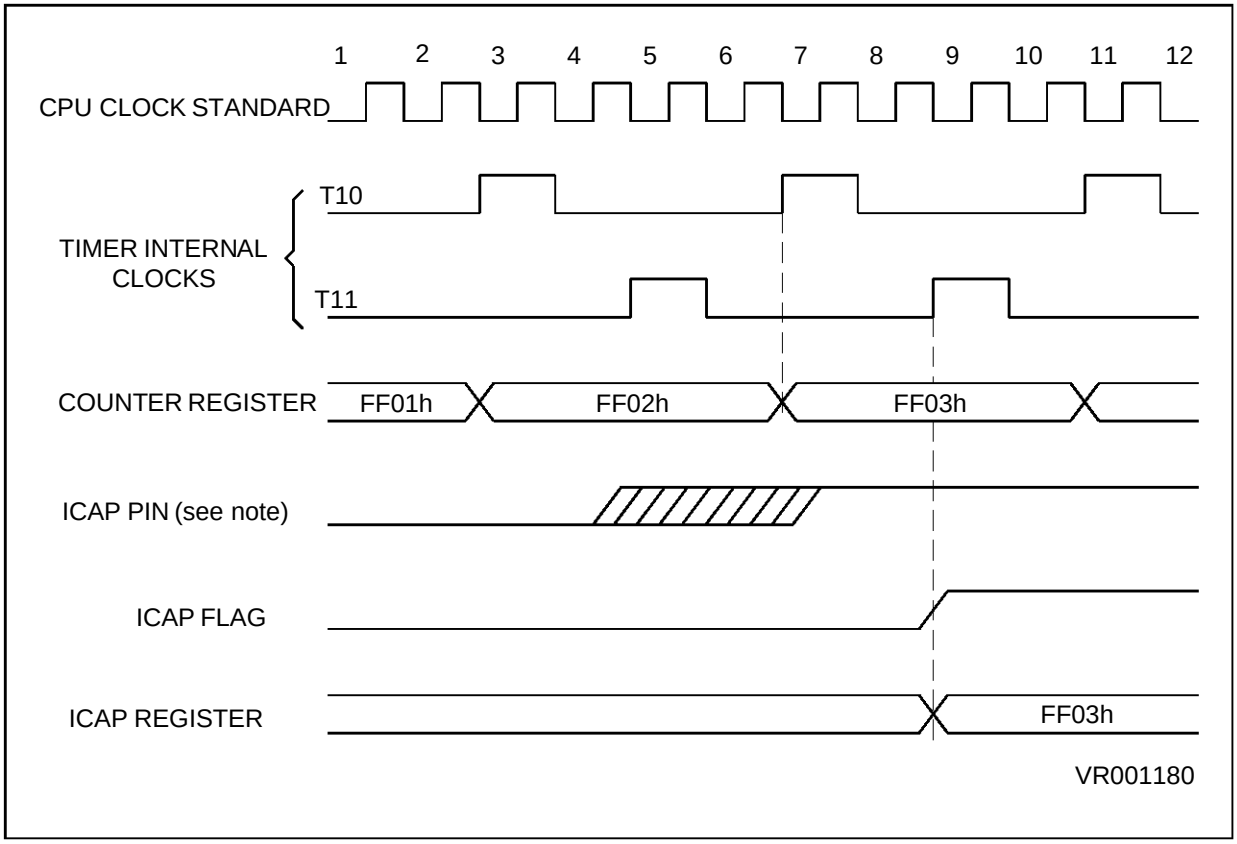
The Output Compare Register 2 (OCR2) is a 16-bit register, which is made up of two 8-bit registers: the most significant byte register (OCHR2) at address 001Eh and the least significant byte register (OCLR2) at address 001Fh.This register works as the Output Compare Register 1. For a complete description, please, refer above in substituting the appropriate index in the bit and register names.

4.3.2.7 Software Force Compare

The force compare capability main purpose is to facilitate fixed frequency generation.

When the Force Output Level 1 bit (FOLV1) of TCR is written to 1, OLVL1 is copied to pin OCMP1. To provide this capability, internal logic allows a single instruction to change OLVL1 and causes a forced compare with the new value of OLVL1. OCF1 is not affected and thus, no interrupt request is generated.

Figure 19. Input Capture Timing Diagram



Note: The Diagram represents a situation with rising edge sensitivity (IEDG1 = 1). The capture operation is performed at the next rising edge of T11, if the action edge of ICAP happened before the previous T10 falling edge.

16 BIT TIMER (Continued)

Figure 20. Timer Timing Diagram.

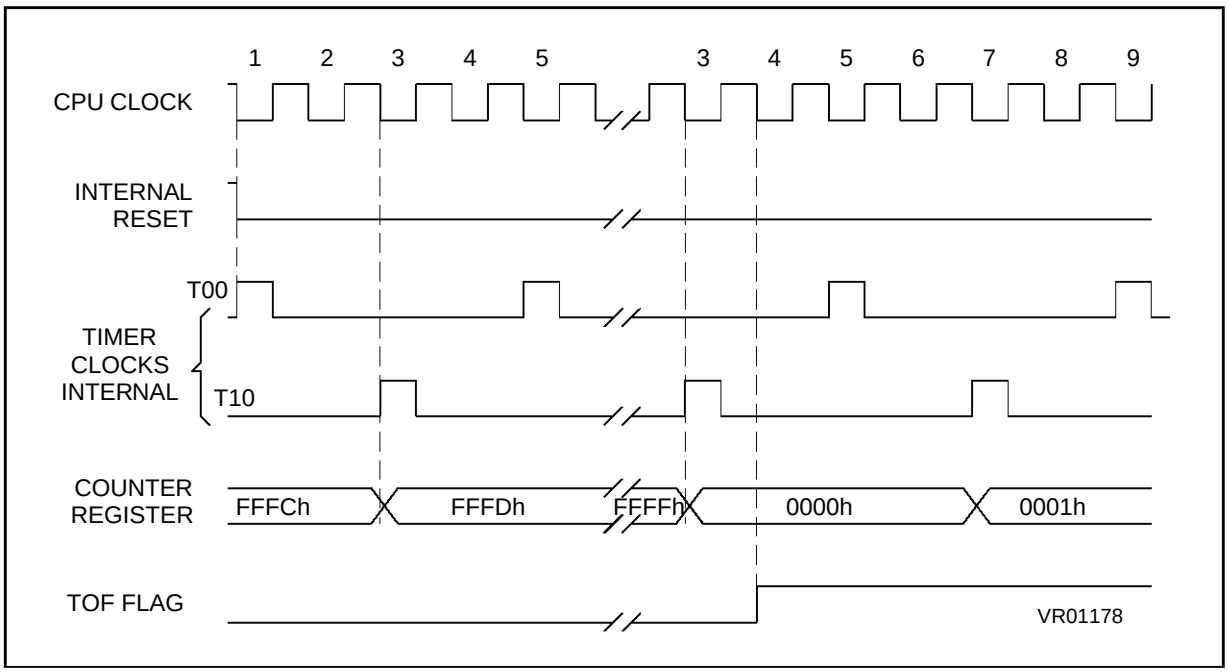
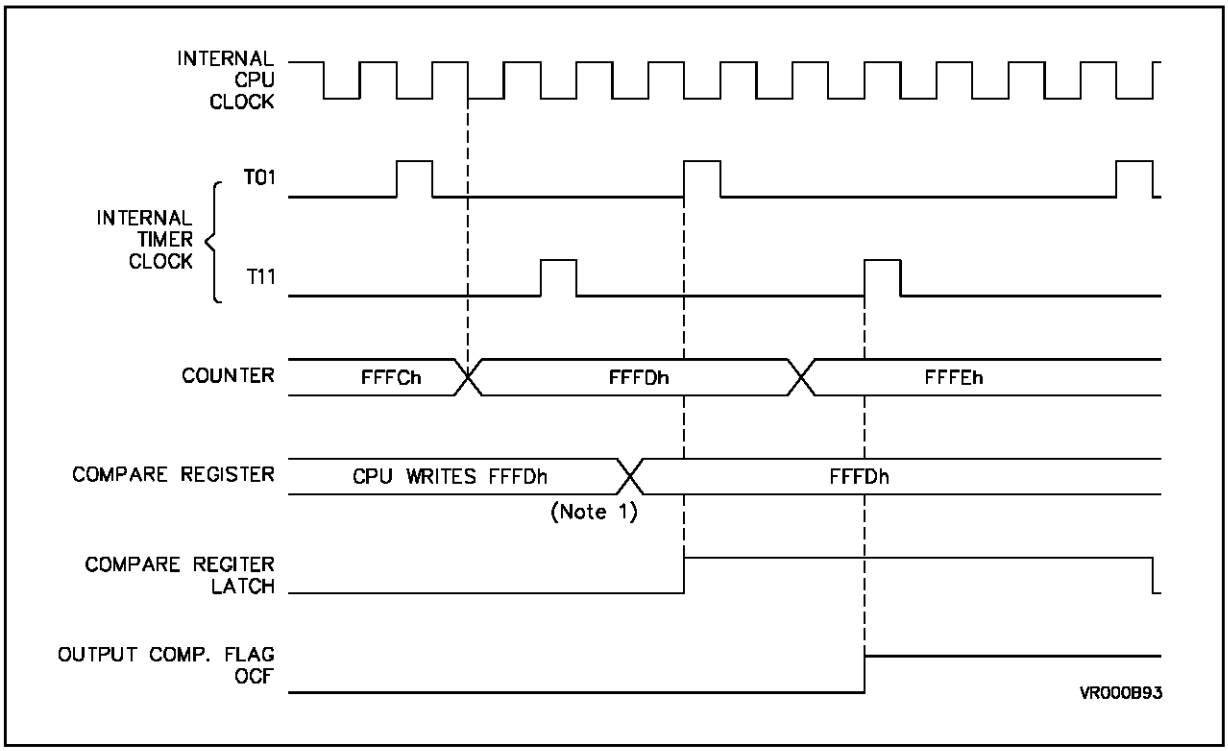


Figure 21. Output Compare Timing Diagram



Note 1: The CPU write to the compare registers may take place at any time but a compare only occurs at timer state T01. Thus a 4-cycle difference may exist between the write to the compare register and the actual compare.

16-BIT TIMER (Continued)

4.3.3 Timer Registers

TIMER CONTROL REGISTER

Register Address: 0012h — Read/Write

Reset Value: 0000 00X0 (00h or 02h)

The TCR is an 8 bit read/write register. Its eight bits are defined as follows:

7							0
ICIE	OCIE	TOIE	-	FOLV1	-	IEDG1	OLVL1

Bit 7 = **ICIE** *Input Capture Interrupt Enable*
If ICIE is set, a timer interrupt is enabled whenever the ICF1 status flags of TSR are set. If the ICIE bit is cleared, the interrupt is inhibited.

Bit 6 = **OCIE** *Output Compare Interrupt Enable*
If OCIE is set, a timer interrupt is enabled whenever the OCF1 or OCF2 status flags of TSR are set. If the OCIE bit is cleared, the interrupt is inhibited.

Bit 5 = **TOIE** *Timer Overflow Interrupt Enable*
If TOIE is set, a timer interrupt is enable whenever the TOF status flag of TSR is set. If the TOIE bit is cleared, the interrupt is inhibited.

Bit 4 = Unused

Bit 3 = **FOLV1** *Force Output Compare 1*
When written to 1, FOLV1 forces OLVL1 to be copied to the OCMP1 pin. FOLV1 has no effect otherwise. It can only be reset by a system reset.

Bit 2 = Unused

Bit 1 = **IEDG1** *Input Edge 1*
The value of the IEDG1 determines which level transition on pin ICAP will trigger a free running counter transfer to the ICR1. When IEDG1 is high, a rising edge triggers the capture since when low, a falling edge does.

Bit 0 = **OLVL1** *Output Level 1*
The OLVL1 bit is copied to the OCMP1 pin whenever a successful comparison occurs at OCR1.

TIMER STATUS REGISTER

Register Address: 0013h — Read Only

Reset Value: Undefined

The Timer Status Register (TSR) is an 8-bit register of which the five most significant bits contain read-only status information and the three least significant bits are not used..

7							0
ICF1	OCF1	TOF	-	0CF2	-	-	-

Bit 7 = **ICF1** *Input Capture Flag 1*
ICF1 is set when a proper edge has been sensed by the input capture edge detector at pin ICAP. The edge is selected by the IEDG1-bit in TCR. ICF1 is cleared by a processor access to the TSR while ICF1 is set followed by an access (read or write) to the low byte of ICR1 (ICLR1).

Bit 6 = **OCF1** *Output Compare Flag 1*
OCF1 is set when the content of the free running counter matches the content of OCR1. It is cleared by a processor access of TSR while OCF1 is set followed by an access (read or write) to the low byte of OCR1.

Bit 5 = **TOF** *Timer Overflow*
TOF is set by a transition of the free running counter from FFFFh to 0000h. It is cleared by a processor access to TSR while TOF is set followed by an access (read or write) to the low byte of the counter low register. TOF is not affected by an access to the Alternate Counter Register.

Bit 4 = Unused

Bit 3 = **OCF2** *Output Compare Flag 2*
OCF2 is set when the content of the free running counter matches the content of OCR2. It is cleared by a processor access of TSR while OCF2 is set followed by an access (read or write) to the low byte of OCR2.

Bit 2, 1, 0 = Unused.

5 SOFTWARE

5.1 ST7 ARCHITECTURE

The 8-bit ST7 Core is designed for high code efficiency. It contains 6 internal registers, 17 main addressing modes and 63 instructions. The 6 internal registers include 2 index registers, an accumulator, a 16-bit Program Counter, a stack pointer and a condition code register. The two Index registers X and Y enable Indexed Addressing modes with or without offset, along with read-modify-write type data manipulations. These registers simplify branching routines and data modifications.

The 16-bit Program Counter is able to address up to 64K of ROM/EPROM memory. The 6-bit Stack Pointer provides access to a 64-level Stack and an upgrade to an 8-bit Stack Pointer is foreseen in order to be able to manage a 256-level Stack. The Core also includes a Condition Code Register providing 5 Condition Flags that indicate the result of the last instruction executed.

The 17 main Addressing modes, including Indirect Relative and Indexed addressing, allow sophisticated branching routines or CASE-type functions. The Indexed Indirect Addressing mode, for instance, permits look-up tables to be located anywhere in the address space, thus enabling very flexible programming and compact C-based code.

The 63-instruction Instruction Set is 8-bit oriented with a 2-byte average instruction size. This Instruction Set offers, in addition to standard data movement and logic/arithmetic functions, byte multiplication, bit manipulation, data transfer between Stack and Accumulator (Push/Pop) with direct stack access, as well as data transfer using the X and Y registers.

5.2 ST7 ADDRESSING MODES

The ST7 Core features 17 different addressing modes which can be classified in 7 main groups:

Addressing Mode	Example
Inherent	nop
Immediate	ld A,#$55
Direct	ld A,$55
Indexed	ld A,($55,X)
Indirect	ld A,([$55],X)
Relative	jrne loop
Bit operation	bset byte,#5

The ST7 Instruction set is designed to minimize the number of bytes required per instruction: To do so, most of the addressing modes may be subdivided in two sub-modes called long and short:

– The long addressing mode is the most powerful because it can reach any byte in the 64kb addressing space, but the instruction is bigger and slower than the short addressing mode.
– The short addressing mode is less powerful because it can generally only access the page zero (00..FF range), but the instruction size is more compact, and faster. All memory to memory instructions are only working with short addressing modes (CLR, CPL, NEG, BSET, BRES, BTJT, BTJF, INC, DEC, RLC, RRC, SLL, SRL, SRA, SWAP)

Both modes have pros and cons, but the programmer doesn't need to choose which one is the best: the ST7 Assembler will always choose the best one.

Table 8. ST7 Addressing Mode Overview:

Mode			Syntax	Destination	Ptr adr	Ptr size	Lgth
Inherent			nop				+ 0
Immediate			ld A,#$55				+ 1
Short	Direct		ld A,$10	00..FF			+ 1
Long	Direct		ld A,$1000	0000..FFFF			+ 2
No Offset	Direct	Indexed	ld A,(X)	00..FF			+ 0
Short	Direct	Indexed	ld A,($10,X)	00..1FE			+ 1
Long	Direct	Indexed	ld A,($1000,X)	0000..FFFF			+ 2
Short	Indirect		ld A,[$10]	00..FF	00..FF	byte	+ 2
Long	Indirect		ld A,[$10.w]	0000..FFFF	00..FF	word	+ 3
Short	Indirect	Indexed	ld A,([$10],X)	00..1FE	00..FF	byte	+ 2
Long	Indirect	Indexed	ld A,([$10.w],X)	0000..FFFF	00..FF	word	+ 3
Relative	Direct		jrne loop	PC+/-127			+ 1
Relative	Indirect		jrne [$10]	PC+/-127	00..FF	byte	+ 2
Bit	Direct		bset $10,#7	00..FF			+ 1
Bit	Indirect		bset [$10],#7	00..FF	00..FF	byte	+ 2
Bit	Direct	Relative	btjt $10,#7,skip	00..FF			+ 2
Bit	Indirect	Relative	btjt [$10],#7,skip	00..FF	00..FF	byte	+ 3

Inherent:

All related instructions are single byte ones. The op-code fully specify all required information for the CPU to process the operation. These instructions are single byte ones.:

Inherent Instruction	Function
NOP	No operation
TRAP	S/W Interrupt
WFI	Wait For Interrupt (Low Power Mode)
HALT	Halt Oscillator (Lowest Power Mode)
RET	Sub-routine Return
IRET	Interrupt Sub-routine Return
SIM	Set Interrupt Mask
RIM	Reset Interrupt Mask
SCF	Set Carry Flag
RCF	Reset Carry Flag
RSP	Reset Stack Pointer
LD	Load
CLR	Clear
PUSH/POP	Push/Pop to/from the stack
INC/DEC	Increment/Decrement
TNZ	Test Negative or Zero
CPL, NEG	1 or 2 Complement
MUL	Byte Multiplication
SLL, SRL, SRA, RLC, RRC	Shift and Rotate Operations
SWAP	Swap Nibbles

Immediate:

The required data byte to do the operation is following the op-code. These are two byte instructions, one for the opcode and the other one for the immediate data byte.

Immediate Instruction	Function
LD	Load
CP	Compare
BCP	Bit Compare
AND, OR, XOR	Logical Operations
ADC, ADD, SUB, SBC	Arithmetic Operations

Direct (short, long):

The data byte required to carry out the operation is found by its memory address, which follows the op-code.

Available Long and Short Direct Instructions	Function
LD	Load
CP	Compare
AND, OR, XOR	Logical Operations
ADC, ADD, SUB, SBC	Arithmetic Additions/Substractions operations
BCP	Bit Compare

Short Direct Instructions Only	Function
CLR	Clear
INC, DEC	Increment/Decrement
TNZ	Test Negative or Zero
CPL, NEG	1 or 2 Complement
BSET, BRES	Bit Operations
BTJT, BTJF	Bit Test and Jump Operations
SLL, SRL, SRA, RLC, RRC	Shift and Rotate Operations
SWAP	Swap Nibbles
CALL, JP	Call or Jump subroutine

The direct addressing mode consists of two sub-modes:

Direct (short):

The address is a byte, thus require only one byte after the op-code, but only allow 00..FF addressing space.

Direct (long):

The address is a word, thus allowing 64Kbytes addressing space, but requires 2 bytes after the op-code.

Indexed (no offset, short, long)

The required data byte to do the operation is found by its memory address, which is defined by the unsigned addition of an index register (X or Y) with an offset which follows the op-code.

No Offset, Long and Short Indexed Instruc.	Function
LD	Load
CP	Compare
AND, OR, XOR	Logical Operations
ADC, ADD, SUB, SBC	Arithmetic Additions/Substractions operations
BCP	Bit Compare

No Offset and Short Indexed Inst. Only	Function
CLR	Clear
INC, DEC	Increment/Decrement
TNZ	Test Negative or Zero
CPL, NEG	1 or 2 Complement
BSET, BRES	Bit Operations
BTJT, BTJF	Bit Test and Jump Operations
SLL, SRL, SRA, RLC, RRC	Shift and Rotate Operations
SWAP	Swap Nibbles
CALL, JP	Call or Jump subroutine

The indirect addressing mode consists of three sub-modes:

Indexed (no offset) :

There is no offset, (no extra byte after the op-code), but only allows 00.FF addressing space.

Indexed (short) :

The offset is a byte, thus require only one byte after the op-code, but only allow 00..1FE addressing space.

Indexed (long) :

The offset is a word, thus allowing 64Kbytes addressing space, but requires 2 bytes after the op-code.

Indirect (short, long):

The required data byte to do the operation is found by its memory address, located in memory (pointer).

Available Long and Short Indirect Instructions	Function
LD	Load
CP	Compare
AND, OR, XOR	Logical Operations
ADC, ADD, SUB, SBC	Arithmetic Additions/Substractions operations
BCP	Bit Compare

Short Indirect Instructions Only	Function
CLR	Clear
INC, DEC	Increment/Decrement
TNZ	Test Negative or Zero
CPL, NEG	1 or 2 Complement
BSET, BRES	Bit Operations
BTJT, BTJF	Bit Test and Jump Operations
SLL, SRL, SRA, RLC, RRC	Shift and Rotate Operations
SWAP	Swap Nibbles
CALL, JP	Call or Jump subroutine

The pointer address follows the op-code. The indirect addressing mode consists of two sub-modes:

Indirect (short) :

The pointer address is a byte, the pointer size is a byte, thus allowing 00..FF addressing space, and requires 1 byte after the op-code.

Indirect (long) :

The pointer address is a byte, the pointer size is a word, thus allowing 64Kbytes addressing space, and requires 1 byte after the op-code.

Indirect Indexed (short, long):

This is a combination of indirect and short indexed addressing mode. The required data byte to do the operation is found by its memory address, which is defined by the unsigned addition of an index register value (X or Y) with a pointer value located in memory. The pointer address follows the op-code.

Long and Short Indirect Indexed Instructions	Function
LD	Load
CP	Compare
AND, OR, XOR	Logical Operations
ADC, ADD, SUB, SBC	Arithmetic Additions/Substractions operations
BCP	Bit Compare

Short Indirect Indexed Instructions Only	Function
CLR	Clear
INC, DEC	Increment/Decrement
TNZ	Test Negative or Zero
CPL, NEG	1 or 2 Complement
BSET, BRES	Bit Operations
BTJT, BTJF	Bit Test and Jump Operations
SLL, SRL, SRA, RLC, RRC	Shift and Rotate Operations
SWAP	Swap Nibbles
CALL, JP	Call or Jump subroutine

The indirect indexed addressing mode consists of two sub-modes:

Indirect Indexed (short) :

The pointer address is a byte, the pointer size is a byte, thus allowing 00..1FE addressing space, and requires 1 byte after the op-code.

Indirect Indexed (long) :

The pointer address is a byte, the pointer size is a word, thus allowing 64Kbytes addressing space, and requires 1 byte after the op-code.

Relative mode (direct, indirect):

This addressing mode is used to modify the PC register value, by adding an 8 bit signed offset to it.

Available Relative Direct/Indirect Instructions	Function
JRxx	Conditional Jump
CALLR	Call Relative

The relative addressing mode consists of two sub-modes:

Relative (direct):

The offset is following the op-code.

Relative (indirect):

The offset is defined in memory, which address follows the op-code.

5.3 ST7 INSTRUCTION SET

The ST7 family devices use an Instruction Set consisting of 63 instructions. The instructions may be subdivided into 13 main groups as illustrated in the following table:

Load and Transfer	LD	CLR						
Stack operation	PUSH	POP	RSP					
Increment/Decrement	INC	DEC						
Compare and Tests	CP	TNZ	BCP					
Logical operations	AND	OR	XOR	CPL	NEG			
Bit Operation	BSET	BRES						
Conditionnal Bit Test and Branch	BTJT	BTJF						
Arithmetic operations	ADC	ADD	SUB	SBC	MUL			
Shift and Rotates	SLL	SRL	SRA	RLC	RRC	SWAP	SLA	
Unconditionnal Jump or Call	JRA	JRT	JRF	JP	CALL	CALLR	NOP	RET
Conditionnal Branch	JRxx							
Interruption management	TRAP	WFI	HALT	IRET				
Code Condition Flag modification	SIM	RIM	SCF	RCF				

Using a pre-byte

The instructions are described with one to four opcodes.

In order to extend the number of available opcodes for an 8-bit CPU (256 op-codes), three different prebyte opcodes are defined. These prebytes modify the meaning of the instruction they precede.

The whole instruction becomes:

PC-2 End of previous instruction

PC-1 Prebyte

PC Op-code

PC+1 Additional word (0 to 2) according to the number of bytes required to compute the effective address

These prebytes enable instruction in Y as well as indirect addressing modes to be implemented. They precede the opcode of the instruction in X or the instruction using direct addressing mode. The prebytes are:

PDY 90 Replace an X based instruction using immediate, direct, indexed or inherent addressing mode by a Y one.

PIX 92 Replace an instruction using direct, direct bit, or direct relative addressing mode to an instruction using the corresponding indirect addressing mode.
It also changes an instruction using X indexed addressing mode to an instruction using indirect X indexed addressing mode.

PIY 91 Replace an instruction using indirect X indexed addressing mode by a Y one.

Table 9. INSTRUCTION SET SUMMARY

Mnemo	Description	Function/Example	Dst	Src	H	I	N	Z	C
ADC	Add with Carry	A = A + M + C	A	M	H		N	Z	C
ADD	Addition	A = A + M	A	M	H		N	Z	C
AND	Logical And	A = A . M	A	M			N	Z	
BCP	Bit compare A, Memory	tst (A . M)	A	M			N	Z	
BRES	Bit Reset	bres Byte, #3	M						
BSET	Bit Set	bset Byte, #3	M						
BTJF	Jump if bit is false (0)	btjf Byte, #3, Jmp1	M						C
BTJT	Jump if bit is true (1)	btjt Byte, #3, Jmp1	M						C
CALL	Call subroutine								
CALLR	Call subroutine relative								
CLR	Clear		reg, M				0	1	
CP	Arithmetic Compare	tst(Reg - M)	reg	M			N	Z	C
CPL	One Complement	A = FFH-A	reg, M				N	Z	1
DEC	Decrement	dec Y	reg, M				N	Z	
HALT	Halt					0			
IRET	Interrupt routine return	Pop CC, A, X, PC			H	I	N	Z	C
INC	Increment	inc X	reg, M				N	Z	
JP	Absolute Jump	jp [TBL.w]							
JRA	Jump relative always								
JRT	Jump relative								
JRF	Never jump	jrf *							
JRIH	Jump if Port B INT pin = 1	(no Port B Interrupts)							
JRIL	Jump if Port B INT pin = 0	(Port B interrupt)							
JRH	Jump if H = 1	H = 1 ?							
JRNH	Jump if H = 0	H = 0 ?							
JRM	Jump if I = 1	I = 1 ?							
JRNM	Jump if I = 0	I = 0 ?							
JRMI	Jump if N = 1 (minus)	N = 1 ?							
JRPL	Jump if N = 0 (plus)	N = 0 ?							
JREQ	Jump if Z = 1 (equal)	Z = 1 ?							
JRNE	Jump if Z = 0 (not equal)	Z = 0 ?							
JRC	Jump if C = 1	C = 1 ?							
JRNC	Jump if C = 0	C = 0 ?							
JRULT	Jump if C = 1	Unsigned <							
JRUGE	Jump if C = 0	Jmp if unsigned >=							
JRUGT	Jump if (C + Z = 0)	Unsigned >							
JRULE	Jump if (C + Z = 1)	Unsigned <=							

Table 9. INSTRUCTION SET SUMMARY

Mnemo	Description	Function/Example	Dst	Src	H	I	N	Z	C
LD	Load	dst <= src	reg, M	M, reg			N	Z	
MUL	Multiply	X,A = X * A	A, X, Y	X, Y, A	0				0
NEG	Negate (2's compl)	neg $10	reg, M				N	Z	C
NOP	No Operation								
OR	OR operation	A = A + M	A	M			N	Z	
POP	Pop from the Stack	pop reg pop CC	reg CC	M M	H	I	N	Z	C
PUSH	Push onto the Stack	push Y	M	reg, CC					
RCF	Reset carry flag	C = 0							0
RET	Subroutine Return								
RIM	Enable Interrupts	I = 0				0			
RLC	Rotate left true C	C <= A <= C	reg, M				N	Z	C
RRC	Rotate right true C	C => A => C	reg, M				N	Z	C
RSP	Reset Stack Pointer	S = Max allowed							
SBC	Substract with Carry	A = A - M - C	A	M			N	Z	C
SCF	Set carry flag	C = 1							1
SIM	Disable Interrupts	I = 1				1			
SLA	Shift left Arithmetic	C <= A <= 0	reg, M				N	Z	C
SLL	Shift left Logic	C <= A <= 0	reg, M				N	Z	C
SRL	Shift right Logic	0 => A => C	reg, M				0	Z	C
SRA	Shift right Arithmetic	A7 => A => C	reg, M				N	Z	C
SUB	Substraction	A = A - M	A	M			N	Z	C
SWAP	SWAP nibbles	A7-A4 <=> A3-A0	reg, M				N	Z	
TNZ	Test for Neg & Zero	tnz lbl1					N	Z	
TRAP	S/W trap	S/W interrupt				1			
WFI	Wait for Interrupt					0			
XOR	Exclusive OR	A = A XOR M	A	M			N	Z	

6 ELECTRICAL CHARACTERISTICS

6.1 ABSOLUTE MAXIMUM RATINGS

The ST7294 device contains circuitry to protect the inputs against damage due to high static voltage or electric fields. Nevertheless, it is recommended that normal precautions be observed and that one should avoid subjecting such high-impedance circuits to voltages higher than those quoted in the Absolute Maximum Ratings, see Table 10. For proper operation, it is recommended that V_{IN} and V_{OUT} be constrained within the range:

$$V_{SS} \leq V_{IN} \text{ and } V_{OUT} \leq V_{DD}$$

To improve reliability, it is recommended that unused I/Os be configured as inputs and that they be connected to an appropriate logic voltage level such as V_{SS} or V_{DD}.

All voltages quoted in the following tables are referenced to V_{SS}.

Stresses above those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 10. Absolute Maximum Rating (Voltage Referenced to V_{SS})

Symbol	Ratings	Value	Unit
V_{DD}	Supply Voltage	-0.3 to +6V	V
V_{IN}	Input Voltage	V_{SS} -0.3 to V_{DD} +0.3	V
IV_{DD} - IV_{SS}	Total current into VSS/VDD pins	50/20	mA
I	Current drain per pin excluding V_{DD} and V_{SS}	20	mA
T_A	Operating Temperature Range (Depending on version)	T_L to T_H 0 to +70 or -40 to +85	°C
T_{STG}	Storage Temperature Range	-65 to +150	°C

6.2 POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in degrees Celsius, may be calculated using the following equation:

$$T_J = T_A + (P_D \times \theta J_A) \quad (1)$$

Where:

– T_A is the Ambient Temperature in °C,

– θJ_A is the Package Junction-to-Ambient Thermal Resistance, in °C/W,

– P_D is the sum of P_{INT} and $P_{I/O}$,

– P_{INT} is the product of I_{CC} and V_{CC}, expressed in Watts. This is the Chip's Internal Power Dissipation.

– $P_{I/O}$ represents the Power Dissipation on Input and Output Pins; User Determined.

For most applications $P_{I/O} < P_{INT}$ and may be neglected. $P_{I/O}$ may be significant if the device is configured to drive Darlington bases or sink LED Loads.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is given by:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Therefore:

$$K = P_D \times (T_A + 273°C) + \theta J_A \times P_D^2 \quad (3)$$

Where:

K is a constant for the particular part, which may be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J may be obtained by solving equations (1) and (2) iteratively for any value of T_A.

Table 11. Thermal Characteristics

Symbol	Characteristics	Value	Unit
θJA	Thermal Resistance PDIP28 PSO28	 55 75	°C/W

6.3 DC ELECTRICAL CHARACTERISTICS (T_A = -40°C to +85°C unless otherwise specified)

Symbol	Test Conditions	Min.	Typ.	Max.	Unit
V_{OL} V_{OH}	Output Voltage, Iload = 10.0µA	V_{DD}-0.1		0.1	V
V_{OH}	Output High Voltage I LOAD =0.8mA, PA0-PA7,PB0-PB7,PC0-PC5	V_{DD}-0.8			V
V_{OL}	Output Low Voltage I LOAD =1.6 mA, PA0-PA7,PB0-PB7,PC0-PC5,$\overline{RESET}$			0.4	V
V_{IH}	Input High Voltage PA0-PA7,PB0-PB7,PC0-PC5, $\overline{INT}$, $\overline{RESET}$	0.7xV_{DD}		V_{DD}	V
V_{IL}	Input Low Voltage PA0-PA7,PB0-PB7,PC0-PC5, $\overline{INT}$, $\overline{RESET}$	V_{SS}		0.2xV_{DD}	V
V_{RM}	Data Retention Mode (0 to 70°C)	2			V
I_{IL}	I/O Ports Hi-Z Leakage Current PA0-PA7,PB0-PB7, PC0-PC5			± 10	µA
I_{IN}	Input Current : $\overline{RESET}$, $\overline{INT}$, ICAP			± 1	µA
C_{OUT}	Capacitance : Ports (as Input or Output)			12	pF
C_{IN}	$\overline{RESET}$, $\overline{INT}$, ICAP			8	pF
R_{PU}	PORT A, B, C (1), V_{DD} = 3.5v, V_{IN} = 0V	125	250	500	kΩ

Note 1. When option is chosen

6.4 AC ELECTRICAL CHARACTERISTICS (T_A = -40°C to +85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{DD}	Operating Supply Voltage	RUN Mode HALT Mode EEPROM Write EEPROM Read	2.5 2.0 3.0 2.5		5.5	V
I_{DD}	Supply Current (1) (2) (3)	RUN Mode V_{DD}=5V,f_{OSC}=4MHz V_{DD}=2.5V,f_{OSC}=1MHz V_{DD}=3.5V,f_{OSC}=455KHz WAIT Mode V_{DD}=5V,f_{OSC}=4MHz V_{DD}=2.5V,f_{OSC}=1MHz V_{DD}=3.5V,f_{OSC}=455KHz HALT MODE V_{DD}=5V,T_A=70°C		 1.8 0.9 1	 2.5 0.4 0.7 1.5 200 500 10	 mA mA mA mA mA mA µA

Notes:

1. RUN (Operating) I_{DD} and WAIT I_{DD} measured using external square wave clock; all inputs 0.2V from rail; no DC load; less than 50pF on all outputs; CI = 20pF on OSC_{out}.
2. WAIT, HALT: all I/Os configured as inputs; V_{IL} = 0.2V, V_{IH} = V_{DD} -0.2V.
3. HALT, OSCin = V_{SS}.

6.5 CONTROL TIMING (T_A = -40°C to +85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
f_{OSC}	Frequency of Operation	V_{DD}=5V V_{DD}=3.0V V_{DD}=2.5V	DC DC DC		4 2 1	MHz
t_{ILCH}	HALT Mode Recovery Startup Time	Crystal Oscillator			50	ms
t_{RL}	External RESET Input Pulse Width		1.5			t_{CYC}
t_{PORL}	Power RESET Output		4096			t_{CYC}
t_{DOGL}	Watchdog RESET Output Pulse Width		1.5			
t_{DOG}	Watchdog Time-out		6144		7168	t_{CYC}
t_{ILIH}	Interrupt Pulse Width INT PORTC		 125 125			ns
t_{ILIL}	Interrupt Pulse Period		(1)			t_{CYC}
t_{OXOV}	Crystal Oscillator Startup Time				50	ms
t_{DDR}	Supply Rise Time	10% to 90%	0.01		100	ms

Note 1. The minimum period t_{ILIL} should not be less than the number of cycle times it takes to execute the interrupt service routine plus 21 cycles.

6.6 EEPROM

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
T_{WEE}	EEPROM Write Time	0 to 70°C		2	8	ms
Endurance	EEPROM Write/Erase Cycles	Q_A Lot Acceptance Criteria	300.000	> 1 million		cycles
Retention	EEPROM Data Retention	T_A = 55°C	10			Years

6.7 TEST CONDITIONS

Details relating to standard test conditions are given in Table 12 below. The standard electrical Test Diagram is shown in Figure 22.

The voltage present on the INT pin determines the device's operating mode, as described in Table 13 below.

CAUTION: *The INT pin is also used to select an internal non-user test mode reserved exclusively for use by* SGS-THOMSON Microelectronics*. This non-user mode is entered on the rising edge of the Reset signal, if:*

– the voltage applied to the INT pin is less than V_{DD} + 0.5V, the device will initialise correctly in User mode;

– if a "high" voltage (typically > V_{DD} + 3V, @ V_{DD} = +5V) is applied to the pin, the device will start in a reserved non-user mode.

Under certain operating conditions apparent device malfunction may be experienced: this may be described as follows:

During the Reset phase, if the V_{DD} supply risetime is slow, the Reset rising edge may occur at a voltage level lower than the minimum allowed voltage of 2.5V. In this case, the "high" voltage which needs to be applied to the INT pin to enter the special mode may be as low as 3.5V, and such a voltage level may be supplied by the external interrupt source, thus provoking an apparent system malfunction.

For this reason it is strongly recommended to manage the INT pin, either by tying it to V_{DD}, if unused, or by connecting it to V_{DD} via a diode, if it is to be used: this will avoid unexpected entry into non-user mode.

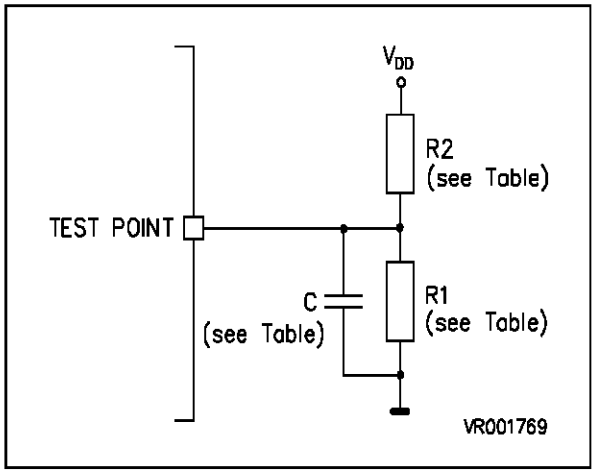
Table 12. Equivalent Test Load

V_{DD} = 3V			
Pins	**R1**	**R2**	**C**
PA0-PA7 PB0-PB7 PC1, PC5, PC6, PC7	10.91kΩ	6.32kΩ	50pF
V_{DD} = 4.5V			
Pins	**R1**	**R2**	**C**
PA0-PA7 PB0-PB7 PC1, PC5, PC6, PC7	3.26kΩ	2.38kΩ	50pF

Table 13. Device Operating Mode Selection

Voltage on INT pin	Operating Mode
V_{DD}	User Mode
V_{SS}	Interrupt
V_{DD} + 3V (typically)	Factory Test

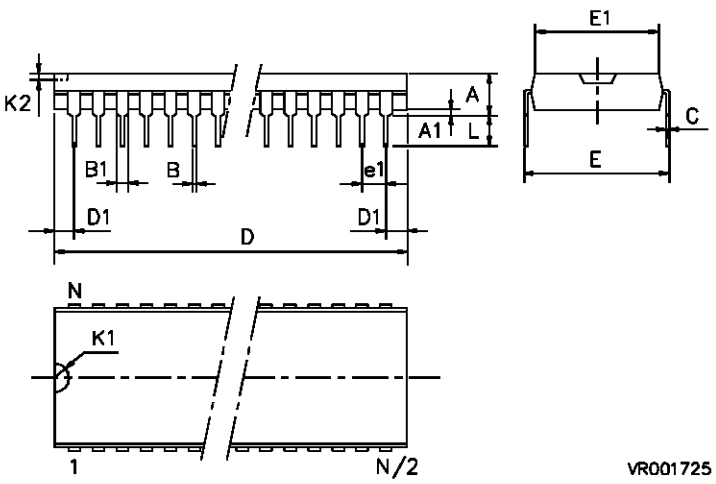
Figure 22. Test Diagram



7 GENERAL INFORMATION

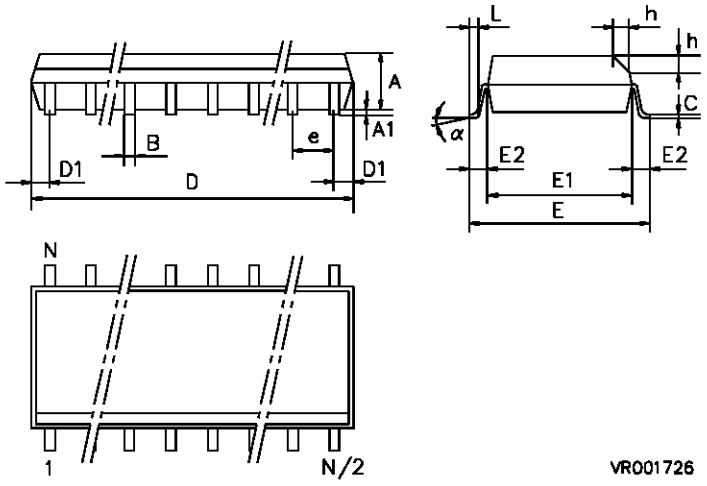
7.1 PACKAGE MECHANICAL DATA

Figure 23. 28-Plastic Dual In Line Package, 600-mil Width



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	2.2		4.8	0.086		0.189
A1	0.51		1.77	0.010		0.069
B	0.38		0.58	0.015		0.023
B1	0.97		1.52	0.055		0.065
C	0.2		0.3	0.008		0.009
D	35.06		36.22	1.400		1.425
D1	–	–	–	–	–	–
E			16.3			0.641
E1		12.9				0.508
K1	–	–	–	–	–	–
K2	–	–	–	–	–	–
L	3.18		4.44	1.25		0.174
e1		2.54			0.10	
	Number of Pins					
N	28					

Figure 24. 28-Lead Small Outline Package, 300-mil Width



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	2.05		2.55	0.081		0.10
A1	0.1		0.3	0.004		.0118
B	0.35		0.49	.0138		.0192
C	0.23		0.32	.0091		.0125
D	17.7		18.1	.6969		.7125
D1	–	–	–	–	–	–
E	10.0		10.65	0.394		0.419
E1	7.40		7.60	.2914		.2992
E2	–	–	–	–	–	–
L	0.40		1.27	0.016		0.050
e1		1.27			0.05	
	Number of Pins					
N	28					

7.2 ORDERING INFORMATION

7.2.1 Introduction

The following section describes the approved procedure for transfer of User Program/Data ROM Code to SGS-THOMSON Microelectronics as well as the basis for contractual agreement with respect to mask programmed devices.

7.2.2 Communication of the User ROM Code

To formally communicate the desired Program/ Data ROM contents to SGS-THOMSON Microelectronics, the following must be supplied:

– a file in MOTOROLA S19 FORMAT (on diskette, via electronic mail or by BBS);

– a correctly completed and signed Option List form as shown overleaf.

The User Code must respect the ROM Memory Map for the selected device option.

The User Code must be generated using an approved ST7 assembler. All unused memory locations shall be set to FFh.

7.2.3 Verification and Formal Approval

When SGS-THOMSON Microelectronics receives the User Code file, it will return a copy of the processed file to the Customer. The Customer will then send formal notification to SGS-THOMSON Microelectronics, approving the file contents. This statement and the file copies to which it refers will then form the basis of the contractual agreement between the Customer and SGS-THOMSON Microelectronics and the agreed file will be used to produce the mask for the programmed MCU device.

The SGS-THOMSON Sales Organization will be pleased to provide detailed information relating to the above technical and contractual points.

Table 14. ORDERING INFORMATION

Sales Types	ROM Size	Temperature Range	Package
ST7294C6B1 ST7294C6M1	6K	0 to +70°C	PDIP28 PSO28
ST7294C6B6 ST7294C6M6		- 40 to +85°C	PDIP28 PSO28

ST7294 STANDARD OPTION LIST

Customer Company . . . . . .
Company Address:. . . . . .
Contact Name: . . . . . .
Phone n°: . . . . . .
Fax n°: . . . . . .

SGS-THOMSON Microelectronics references:

Package:	[ ] PSO28	[ ] PDIP28
Conditioning (if PSO package):	[ ] Tape & Reel	[ ] Stick (Standard)
Temperature Range:	[ ] 0 to 70°C	[ ] -40 to 85°C

Special marking is available on one line with up to 11 characters
Special Marking [ ] (y/n) " _ _ _ _ _ _ _ _ _ _ _ "
Authorized characters are letters, digits, ' . ', ' - ', ' / ' and spaces.

OPTIONS:

Watchdog ENABLE MODE	[ ] Software Enable	[ ] Always Enable
Watchdog during WAIT	[ ] Active during WAIT mode	[ ] Suspend during WAIT mode
Enable Wake-up on PORT C	[ ] PORT C 6-bit I/O PORT [ ] PORT C interrupt Wake-up inputs	
Pinout for ICAP (PC0)	[ ] ICAP bonded to pin 18 [ ] PC0 bonded to pin 18	
Pinout for OCMP1 (PC1)	[ ] OCMP1 bonded to pin 17 [ ] PC0 bonded to pin 17	
PORT A Outputs	[ ] Standard Push-Pull output PORT [ ] Open-Drain output PORT	
PORT A Pull-ups	[ ] No Pull-up [ ] Pull-up when a line is defined as an input	
PORT B Pull-ups	[ ] No Pull-up [ ] Pull-up when a line is defined as an input	

Yearly quantity forecast:	[.....] K Units
For a period of	[.....] Years
Preferred production start dates:	[.....] (YY/MM/DD)
Risk order quantity:	[.....]
Agreed A.S.P.	[.....]

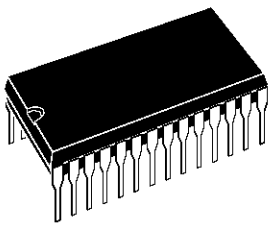
Signature . . . . . .
Date . . . . . .

SGS-THOMSON MICROELECTRONICS

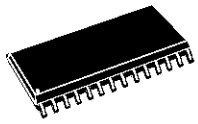
ST72E94
ST72T94

8-BIT HCMOS MCU WITH 6K EPROM, EEPROM AND 16-BIT TIMER WITH INPUT CAPTURE AND OUTPUT COMPARE

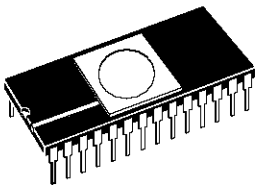
- 3.0 to 5.5V Supply Operating Range
- 4MHz Maximum Clock Frequency
- Fully Static operation
- -40° to +85°C Operating Temperature Range
- Run, Wait, Stop and RAM Retention modes
- User EPROM: 6,144 bytes
- Data RAM: 224 bytes
- EEPROM: 256 bytes
- 28 pin Dual-in-Line and SO plastic packages for ST72T94 OTP version
- 28 pin Ceramic Dual-in-Line package for ST72E94 EPROM version
- 22 Bidirectional I/O lines
- 6 Interrupt Wake-Up programmable input lines
- 16-bit Timer with Input Capture and dual Output Compare
- 2V RAM Data Retention mode
- Master Reset and Power-On Reset
- Compatible with ST7294 (6K) and ST7293 (3.25K) ROM devices
- 8-bit Data Manipulation
- 63 Basic Instructions
- 17 main Addressing Modes
- 8x8 Unsigned Multiply instruction
- True Bit Manipulation
- Complete Development Support on PC/DOS Real-Time Emulator
- Full Software Package (Cross-Assembler, Debugger)



PDIP28



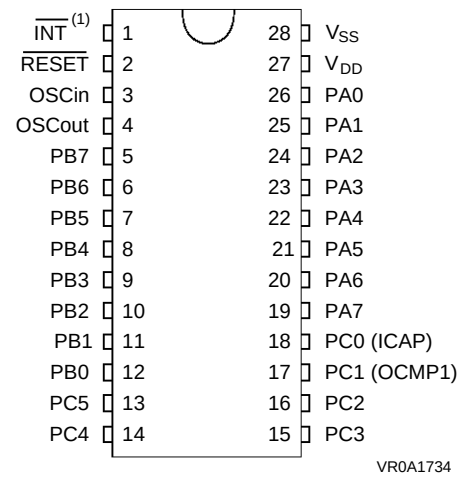
PSO28



CDIP28W

(See end of Datasheet for Ordering Information)

Figure 1. Pin Description



Note 1. This pin is also the V_{PP} input for EPROM based devices

1 GENERAL DESCRIPTION

1.1 INTRODUCTION

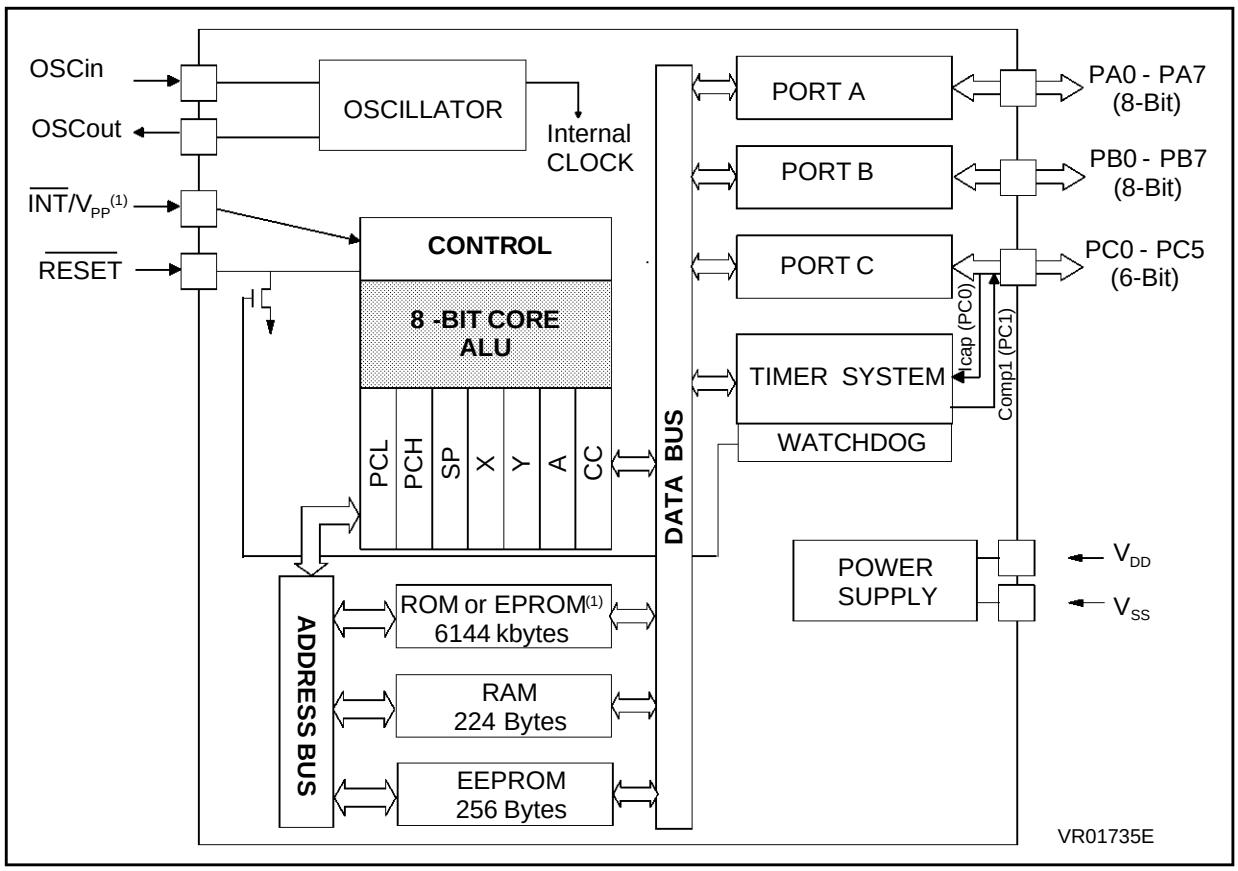
The ST72E94 and ST72T94 (following mentioned as ST72E94) are EPROM members with EEPROM of the ST72 family of microcontrollers, in windowed ceramic (E) and plastic OTP (T) packages respectively, completely developed and produced by SGS-THOMSON Microelectronics using a n-well proprietary HCMOS process. The EPROM parts are fully compatible with their ROM versions and this datasheet will thus provide only information specific to the EPROM based devices.

THE READER IS ASKED TO REFER TO THE DATASHEET OF THE ST7294 AND ST7293 ROM-BASED DEVICES FOR FURTHER DETAILS.

The ST72E94 is an user-programmable and erasable device. It is best suited for development. The ST72T94 is a One-Time Programmable device (OTP). It offers the best cost/flexibility trade-off for prototyping and preseries as well as most low to medium volume applications.

The ST72E94 and ST72T94 are HCMOS microcontrollers from the ST72 family. They are based around an 8-bit core industry standard and offers an enhanced instruction set. The processor runs with an external clock at 4 MHz with a 5V supply and 2MHz with a 3V supply. Due to the fully static design of this device, operation down to DC is possible. Under software control the ST72E94 and ST72T94 can be placed in WAIT or HALT mode thus reducing power consumption. The enhanced instruction set and addressing modes afford real programming potential. In addition to standard 8 bit data management the ST72E94 and ST72T94 feature true bit manipulation, 8x8 unsigned multiplication and indirect addressing modes. The devices include an on-chip oscillator, CPU, EPROM, RAM, EEPROM, I/O, and one timer with 1 input capture and 2 output compare systems.

Figure 2. ST72E94 Block Diagram



Note 1. EPROM version only

1.2 PIN DESCRIPTION

V_{DD}. Power supply.

V_{SS}. Ground.

OSCin, OSCout. Oscillator input and output pins. These pins are to be connected to a parallel resonant crystal or ceramic resonator. An external clock source can also be input through OSCin.

$\overline{\text{RESET}}$. The active low input signal forces the initialisation of the MCU. This event is the first priority interrupt. This pin is switched output low when the Watchdog has released. It could be used to reset external peripherals.

$\overline{\text{INT}}$/V_{PP}. is the external interrupt signal. Software configuration allows four triggering modes. In the EPROM programming mode, this pin acts as the programming voltage input V_{PP}.

ICAP (PC0). Input capture signal going to the TIMER system. This signal, according to a mask option, can be an ICAP pin or PC0 pin. When PC0 is defined as ICAP, the internal pull-up resistor is not connected.

OCMP1 (PC1). Output compare signal coming from the TIMER system. This output signal, according to a mask option, can be an OCMP1 pin (for output compare 1 of the timer) or PC1 pin. When PC1 is defined as OCMP1, the internal pull-up resistor is not connected.

PA0-PA7, PB0-PB7, PC0-PC5. These 22 lines are standard I/O lines, programmable as either input or output.

– PORT A. 8 Standard I/O lines, bit programmable, accessed through DDRA and DRA Registers. According to a mask option, the outputs can be defined as a standard push-pull output port or as an open drain output port. According to another mask option, a pull-up resistor can be added on each line when it is defined as an input.

– PORT B. 8 Standard I/O lines bit programmable accessed through DDRB and DRB Registers. According to another mask option, a pull-up resistor can be added on each line when it is defined as an input.

– PORT C. 6 Standard I/O lines accessed through DDRC and DRC Registers. According to a mask option, these 6 lines can become 6 falling edge sensitive interrupt lines all linked to a single interrupt vector or 6 standard input ports tied to V_{DD} through an internal pull-up resistor. These negative edge sensitive interrupt lines can wake-up the ST72E94 from WAIT or HALT mode. This feature allows to build low power applications when the ST72E94 can be waken-up from keyboard push.

PIN DESCRIPTION (Continued)

Table 1. ST72E94 Pin Configuration

Name	Function	Description	Pin Assignment
$\overline{INT}/V_{PP}$	I	Interrupt / EPROM Programming Voltage	1
$\overline{RESET}$	I/O	Reset	2
OSCin	I	Oscillator	3
OSCout	O	Oscillator	4
PB7	I/O	Standard Port (bit programmable)	5
PB6	I/O	Standard Port (bit programmable)	6
PB5	I/O	Standard Port (bit programmable)	7
PB4	I/O	Standard Port (bit programmable)	8
PB3	I/O	Standard Port (bit programmable)	9
PB2	I/O	Standard Port (bit programmable)	10
PB1	I/O	Standard Port (bit programmable)	11
PB0	I/O	Standard Port (bit programmable)	12
PC5	I/O	Standard Port (falling edge interrupt line)	13
PC4	I/O	Standard Port (falling edge interrupt line)	14
PC3	I/O	Standard Port (falling edge interrupt line)	15
PC2	I/O	Standard Port (falling edge interrupt line)	16
PC1 (OCMP1)	I/O	Standard Port (falling edge interrupt line or timer output compare)	17
PC0 (ICAP)	I/O	Standard Port (falling edge interrupt line or timer input capture)	18
PA7	I/O	Standard Port (bit programmable)	19
PA6	I/O	Standard Port (bit programmable)	20
PA5	I/O	Standard Port (bit programmable)	21
PA4	I/O	Standard Port (bit programmable)	22
PA3	I/O	Standard Port (bit programmable)	23
PA2	I/O	Standard Port (bit programmable)	24
PA1	I/O	Standard Port (bit programmable)	25
PA0	I/O	Standard Port (bit programmable)	26
V_{DD}	I/O	Power Supply	27
V_{SS}	I/O	Ground	28

1.3 MEMORY MAP

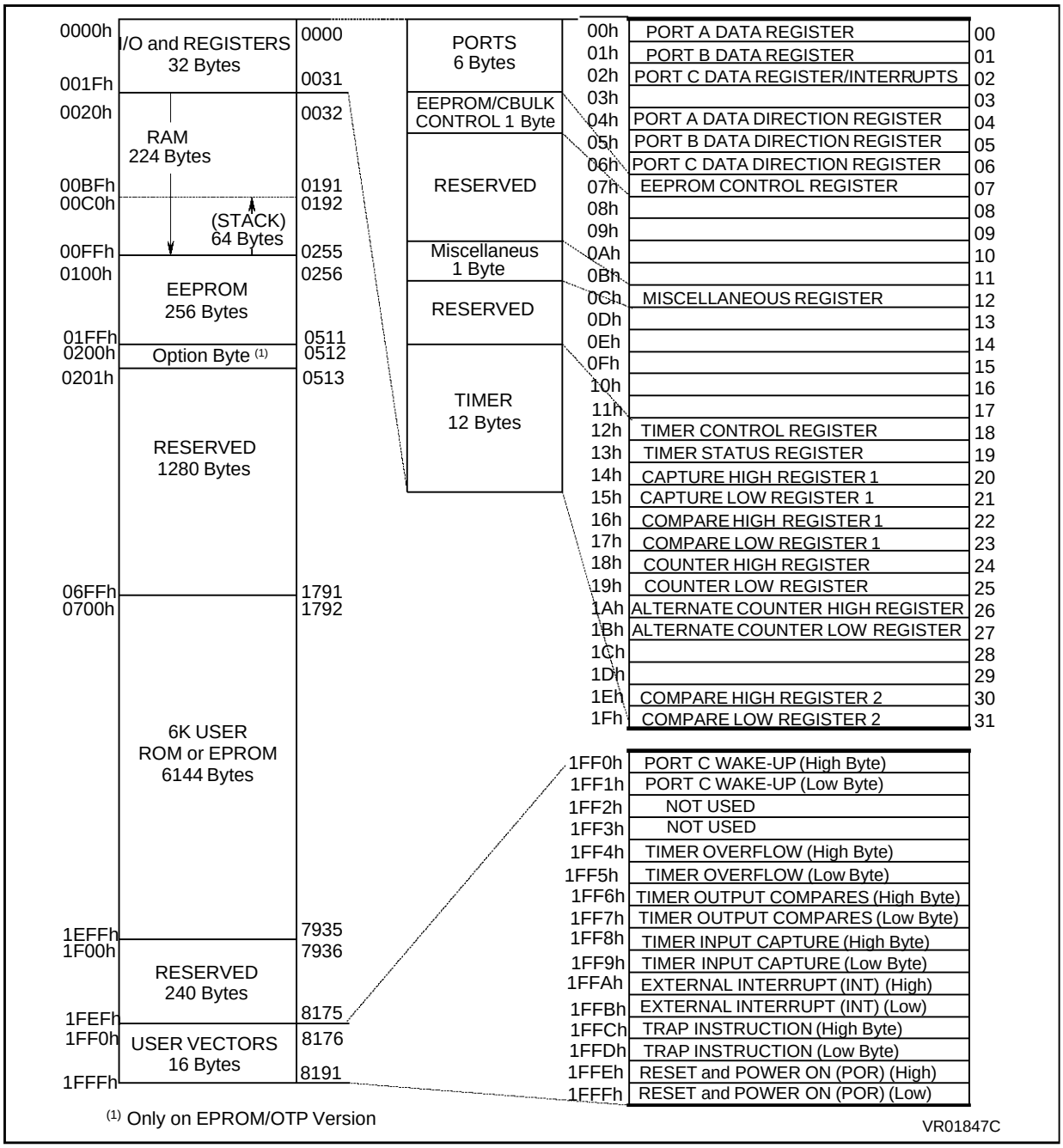
As shown in Figure 3, the MCU is capable of addressing 8192 bytes of memory and I/O registers. In the ST72E94, 7696 of these bytes are user accessible.

Note:
In the ST7293 only 3.25K bytes are user accessible. This should be taken into account by the user when programming the ST72E94 to emulate the ST7293.

The locations consist of 32 bytes of I/O registers (only 20 are used), 224 bytes of RAM, 256 bytes of EEPROM and 6Kbytes of user ROM. The RAM space includes 64 bytes for the stack from 0FFh to 0C0h. Programs that only use a small part of the allocated stack locations for interrupts and/or subroutine stacking purpose can use the remaining bytes as standard RAM locations.

The highest address bytes contains the user defined reset and interrupt vectors.

Figure 3. Memory Map



1.4 OPTION BYTE

An additional mode is used to configure the part for programming of the EPROM. This is set by a +12.5 voltage applied to the $\overline{INT}/V_{PP}$.

The EPROM memory may be programmed by using the EPROM Programming Boards (EPB) available from SGS-THOMSON.

The ROM devices of the ST72 family can be configured through mask options. In EPROM devices, most mask options are replaced by EPROM bits grouped in the Option Byte. The configuration of the device is made by programming the Option Byte.

The Option Byte is not in the user memory space. The Option Byte is accessed only if the device is in programming mode and location 0200h is addressed. The EPB provides all the functionality to select and program the Option Byte.

7							0
WIW	WDMS	PBIP	PCWS	PC1S	PC0S	PA0S	PAIP

b7 = **WIW**: *Watchdog in Wait.*
1 : Watchdog suspended during Wait
0 : Watchdog active during Wait

b6 = **WDMS**: *Watchdog Enable Mode*.
1 : Watchdog in Software Select Mode
0 : Watchdog in auto-enable Mode

b5 = **PBIP**: *Port B Input Pull-up.*
1 : Pull-up enabled or Port B (when Input)
0 : No Pull-up on Port B

b4 = **PCWS**: *Port C Wake-up Select.*
1 : Port C I/O functions enabled
0 : Port C Interrupt Wake-up Inputs enabled

b3 = **PC1S**: *PC1 Select.*
1 : Timer OCMP1 connected to pin 17
0 : PC1 I/O function connected to pin 17

b2 = **PC0S**: *PC0 Select.*
1 : Timer ICAP connected to pin 18
0 : PC0 I/O function connected to pin 18

b1 = **PA0S**: *Port A Output Select*.
1 : Port A Output is Push-pull
0 : Port A Output is Open-drain

b0 = **PAIP**: *Port A Input Pull-up.*
1 : Pull-up enabled on Port A (when Input)
0 : No Pull-up on Port A

1.5 EPROM ERASURE (ST72E94 ONLY)

The ST72E94 is erased by exposure to high intensity UV light through the transparent window. This exposure discharges the floating gate to its initial state through induced photo current.

It is recommended that the ST72E94 be kept out of direct sunlight because the UV content of sunlight can cause temporary functional failure. Extended exposure to room level fluorescent lighting will also cause erasure. An opaque coating (paint, tape, label, etc...) should be placed over the package window if the product is to be operated under these lighting conditions. Covering the window also reduces IDD in stop mode due to photo diode currents.

An Ultraviolet source of wave length 2537 Å yielding a total integrated dosage of 15 Watt-sec/cm is required to erase the ST72E94. This device will be erased in 15 to 20 minutes if an UV lamp with a 12mW/cm power rating is placed 1 inch from the lamp without filters.

1.6 VOLTAGE RANGE

The ST72E94 and ST72T94 operate with a minimum supply voltage of 3.0V when the ST7294 operates from 2.5V.

2 ELECTRICAL CHARACTERISTICS

2.1 ABSOLUTE MAXIMUM RATINGS

The ST72E94/T94 devices contain circuitry to protect the inputs against damage due to high static voltage or electric field. Nevertheless it is advised to take normal precautions and to avoid applying to this high impedance voltage circuit any voltage higher than the maximum rated voltages. It is recommended for proper operation that V_{IN} and V_{OUT} be constraint to the range:

$$V_{SS} \leq V_{IN} \text{ and } V_{OUT} \leq V_{DD}$$

To enhance reliability of operation, it is recommended to configure unused I/Os as inputs and to connect them to an appropriate logic voltage level such as V_{SS} or V_{DD}.

All the voltage in the following tables are referenced to V_{SS}.

Stresses above those listed as “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Rating (Voltage Referenced to V_{SS})

Symbol	Ratings	Value	Unit
V_{DD}	Supply Voltage	-0.3 to +6V	V
V_{IN}	Input Voltage	V_{SS} -0.3 to V_{DD} +0.3	V
IV_{DD} - IV_{SS}	Total current into VSS/VDD pins	50/20	mA
I	Current drain per pin excluding V_{DD} and V_{SS}	20	mA
T_A	Operating Temperature Range	T_L to T_H 0 to +70	°C
T_{STG}	Storage Temperature Range	-65 to +150	°C

2.2 POWER CONSIDERATIONS

T_J, the average chip-junction temperature in Celsius can be calculated from the following equation:

$$T_J = T_A + (P_D \times \theta J_A) \quad (1)$$

Where:

– T_A is the Ambient Temperature in °C,

– θJ_A is the Package Thermal Resistance, Junction-to-Ambient in °C/W,

– P_D the sum of P_{INT} and $P_{I/O}$,

– P_{INT} equals I_{CC} time V_{CC}, Watts-Chip Internal Power

– $P_{I/O}$ the Power Dissipation on Input and Output Pins, User Determined.

For most applications $P_{I/O} < P_{INT}$ and can be neglected.

$P_{I/O}$ may be significant if the device is configured to drive Darlington bases or sink LED Loads.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Therefore:

$$K = P_D \times (T_A + 273°C) + \theta J_A \times P_D^2 \quad (3)$$

Where K is constant pertaining to the particular part, K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

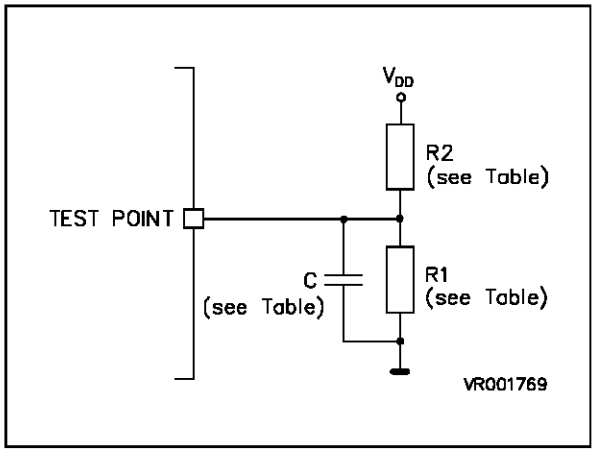
Thermal Characteristics

Symbol	Characteristics	Value	Unit
θJA	Thermal Resistance PDIP28 PSO28	 55 75	°C/W

Equivalent Test Load

V_{DD} = 3V			
Pins	**R1**	**R2**	**C**
PA0-PA7 PB0-PB7 PC0-PC5	10.91kΩ	6.32kΩ	50pF
V_{DD} = 4.5V			
Pins	**R1**	**R2**	**C**
PA0-PA7 PB0-PB7 PC0-PC5	3.26kΩ	2.38kΩ	50pF

Test Diagram



2.3 DC ELECTRICAL CHARACTERISTICS (T_A = -40°C to +85°C unless otherwise specified)

Symbol	Test Conditions	Min.	Typ.	Max.	Unit
V_{OL} V_{OH}	Output Voltage, Iload 10.0µA	 V_{DD}-0.1		0.1	V
V_{OH}	Output High Voltage I LOAD =0.8mA, PA0-PA7,PB0-PB7,PC0-PC5	V_{DD}-0.8			V
V_{OL}	Output Low Voltage I LOAD =1.6 mA, PA0-PA7,PB0-PB7,PC0-PC5,$\overline{\text{RESET}}$			0.4	V
V_{IH}	Input High Voltage PA0-PA7,PB0-PB7,PC0-PC5, $\overline{\text{INT}}$, $\overline{\text{RESET}}$	0.7xV_{DD}		V_{DD}	V
V_{IL}	Input Low Voltage PA0-PA7,PB0-PB7,PC0-PC5, $\overline{\text{INT}}$, $\overline{\text{RESET}}$	V_{SS}		0.2xV_{DD}	V
V_{RM}	Data Retention Mode (0 to 70°C)	2			V
I_{IL}	I/O Ports Hi-Z Leakage Current PA0-PA7,PB0-PB7, PC0-PC5			± 10	µA
I_{IN}	Input Current: $\overline{\text{RESET}}$, $\overline{\text{INT}}$, ICAP			± 1	µA
C_{OUT}	Capacitance: Ports (as Input or Output)			12	pF
C_{IN}	$\overline{\text{RESET}}$, $\overline{\text{INT}}$, ICAP			8	pF
R_{PU}	PORT A, B, C (1), V_{DD} = 3.5V, V_{IN} = 0V	125	250	500	kΩ

Note 1. When option is chosen

2.4 AC ELECTRICAL CHARACTERISTICS (T_A = -40°C to +85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{DD}	Operating Supply Voltage	RUN Mode HALT Mode EEPROM Write EEPROM Read	3.0 2.0 3.0 3.0		5.5	V
I_{DD}	Supply Current (1) (2) (3)	RUN Mode V_{DD}=5V,f_{OSC}=4MHz V_{DD}=3.0V,f_{OSC}=455KHz WAIT Mode V_{DD}=5V,f_{OSC}=4MHz V_{DD}=3.0V,f_{OSC}=455KHz HALT MODE V_{DD}=5V,T_A=70°C		 1.8 0.9 1	 2.5 0.7 1.5 500 10	 mA mA mA mA µA

Notes:

1. RUN (Operating) IDD, WAIT I_{DD} measured using external square wave clock all inputs 0.2V from rail, no DC load, less than 50pF on all outputs, CI = 20pF on OSCout.
2. WAIT, HALT all I/O configured as inputs, V_{IL} = 0.2V, V_{IH} = V_{DD} -0.2V.
3. HALT, OSCin = V_{SS}.

2.5 Control Timing (T_A = -40°C to +85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
f_{OSC}	Frequency of Operation	V_{DD}=5V V_{DD}=3.0V	DC DC		4 2	MHz
t_{ILCH}	HALT Mode Recovery Startup Time	Crystal Oscillator			50	ms
t_{RL}	External RESET Input Pulse Width		1.5			t_{CYC}
t_{PORL}	Power RESET Output		4096			t_{CYC}
t_{DOGL}	Watchdog RESET Output Pulse Width		1.5			
t_{DOG}	Watchdog Time-out		6144		7168	t_{CYC}
t_{ILIH}	Interrupt Pulse Width INT PORTC		 125 125			ns
t_{ILIL}	Interrupt Pulse Period		(1)			t_{CYC}
t_{OXOV}	Crystal Oscillator Startup Time				50	ms
t_{DDR}	Supply Rise Time	10% to 90%	0.01		100	ms

Note 1. The minimum period t_{ILIL} should not be less than the number of cycle times it takes to execute the interrupt service routine plus 21 cycles.

2.6 EEPROM

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
T_{WEE}	EEPROM Write Time	0 to 70°C		2	8	ms
Endurance	EEPROM Write/Erase Cycles	Q_A Lot Acceptance Criteria	300.000	> 1 million		cycles
Retention	EEPROM Data Retention	T_A = 55°C	10			Years

3 GENERAL INFORMATION

SGS-THOMSON offers ST7 devices in EPROM and OTP as well as in the ROM version. This range of product options provides the ST7 user with maximum of flexibility for his application needs.

The OTP rather than the ROM version of the ST7 is recommended when the customer's quantity requirement is relatively small on a given code - e.g. less than 10 thousand pieces. But the OTP solution is also popular even for volumes when the customer has a need for reduced leadtime, whether pre-production, an unforecasted increase in demand, or a quick program change. And the OTP is often preferred by those customers who have several codes running concurrently since they need purchase and stock only one vendor sales type.

However, it must be understood that the ROM and OTP follow different production flows and that the difference between these flows, in particular the method by which final electrical test is performed, may have an impact on the customer.

The basic production flow is as follows:

– Wafer diffusion

– Electrical test of dice (wafer sort)

– Assembly (encapsulation)

– Final electrical test

For ROM parts, the customer program is included at a specific mask of the wafer. Therefore, all of the product's functionality is present in both the die and the assembled product and this functionality can be fully evaluated at both wafer sort and final electrical test. SGS-THOMSON fully tests the ROM version's functionality at both wafer sort and final test, thus ensuring conformance to the electrical specification and a low reject rate.

But for OTPs there exists an additional feature that must be tested: programmability.The program memory of an OTP should be seen as a collection of fuses that will be blown during programming. These fuses can be "recovered" by lightening the die with UV light. This recovery is no longer possible once the OTP die has been encapsulated in an opaque plastic package. The programmability and data retention can only be fully tested at wafer sort.

At this step the dice are electrically tested and the memory is programmed to verify programmability. Then the wafers are placed in high temperature bake in order to provoke any possible memory retention defects. They are then retested to check data retention. After this test, UV light is used to "recover" the fuses and the good dice are assembled.

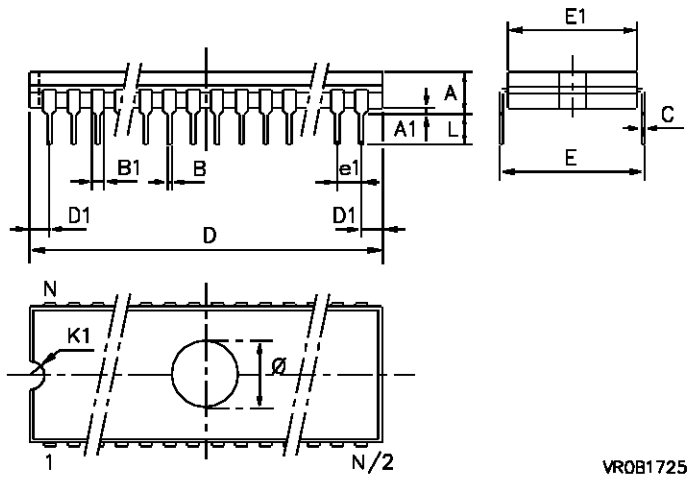
Although the programmability of the OTP dice is verified as fully functional at probe test, the die encapsulation process has the potential to affect this function in the finished product. It is therefore necessary that in addition to electrical final test, a programmability test be made. However since UV light cannot be used to erase an OTP's programmed byte once the die has been encapsulated it is then impossible to write a test pattern and thus to check 100% of the user program area. For this reason the final test is limited to a reserved number of bytes which are programmed and then verified.

As the programmability of the OTP cannot be fully tested once the die has been encapsulated, unlike the ROM or EPROM versions, a customer should find a programming reject rate below 1.0% and a data retention reject rate below 0.5% when programming is performed using qualified programming tools. Apart from the programmability, the OTP has the same reject as EPROM and ROM versions.

In order to lower the reject levels for programmability and data retention, SGS-THOMSON is continually pursuing technology improvements in areas such as soft die handling, low stress compounds, and passivation layer enhancements.

3.1 PACKAGE MECHANICAL DATA

Figure 4. 28-Ceramic Dual In Line Package, 600-mil Width



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			5.71			0.225
A1	0.50		1.78	0.020		0.070
B	0.40		0.55	0.016		0.022
B1	1.17		1.42	0.046		0.056
C	0.22		0.31	0.009		0.012
D			38.10			1.50
D1	1.52		2.49	0.060		0.098
E	-	-	-	-	-	-
E1	13.05		13.36	0.514		0.526
L	3.00			0.118		
e1	2.29		2.79	0.090		0.110
∅	6.86		7.36	0.270		0.290
	Number of Pins					
N	28					

3.2 ORDERING INFORMATION

ORDERING INFORMATION TABLE

Sales Types	ROM Size	Temperature Range	Package
ST72T94C6B6	6K	-40°C to +85°C	PDIP28
ST72T94C6M6			PSO28
ST72E94C6F0		25°C	CDIP28

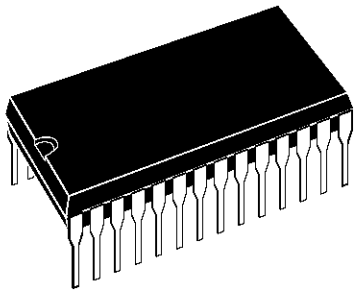
Notes:

SGS-THOMSON MICROELECTRONICS

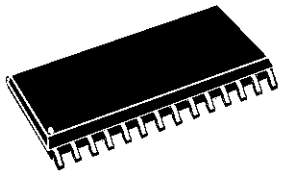
ST7293

8-BIT MCU WITH 3K ROM, EEPROM AND 16-BIT TIMER WITH INPUT CAPTURE AND DUAL OUTPUT COMPARE

- 2.5 to 5.5V Supply Operating Range
- 4MHz Maximum Clock Frequency
- Fully Static operation
- -40° to +85°C Operating Temperature Range
- Run, Wait, Stop and RAM Retention modes
- User ROM: 3,328 bytes
- Data RAM: 128 bytes
- EEPROM: 128 bytes
- 28 pin Dual-in-Line and SO plastic packages
- 22 Bidirectional I/O lines
- 6 Interrupt Wake-Up programmable input lines
- 16-bit Timer with Input Capture and dual Output Compare
- 2V RAM Data Retention mode
- Master Reset and Power-On Reset
- Maskable Options for:
  - Input Capture (ICAP) and Output Compare (OCMP) signal pinouts
  - PORT C Wake-Up function
  - PORT A Open-Drain outputs
  - PORTS A and B input Pull-Ups
  - Watchdog Enabled/Disabled following Reset
  - Watchdog Enabled during WAIT mode
- 8-bit Data Manipulation
- 63 Basic Instructions
- 17 main Addressing Modes
- 8x8 Unsigned Multiply instruction
- True Bit Manipulation
- Complete Development Support on PC/DOS Real-Time Emulator
- Full Software Package (Cross-Assembler, Debugger)
- EPROM and OTP support



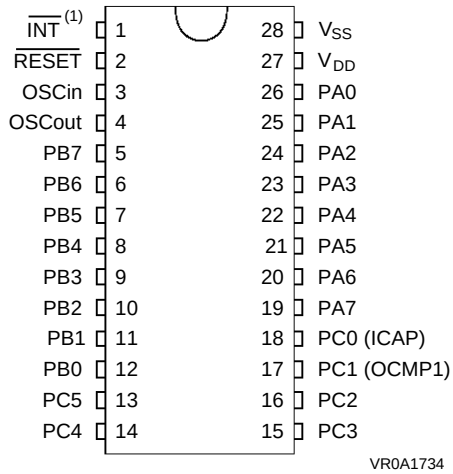
PDIP28



PSO28

(See end of Datasheet for Ordering Information)

Figure 1. Pin Description



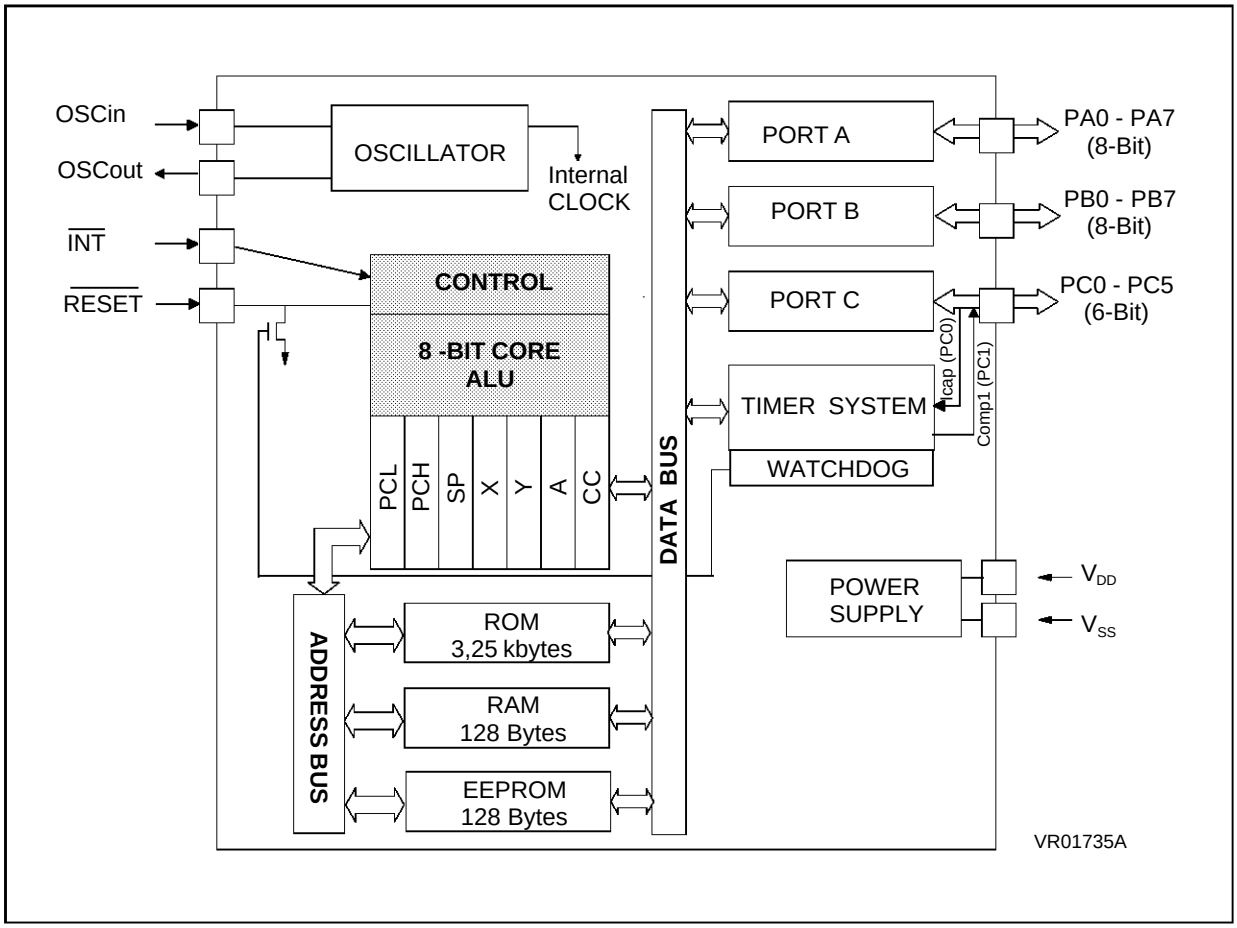
Note 1. This pin is also the V_{PP} input for EPROM based device

1 GENERAL DESCRIPTION

1.1 INTRODUCTION

The ST7293 is a HCMOS microcontroller unit (MCU) from the ST7 family. It is based around an industry standard 8 bit core and offers an enhanced instruction set. The processor runs with an external clock at 8MHz with a 5V supply and 4MHz with a 3.0V supply. Due to the fully static design of this device, operation down to DC is possible. Under software control the ST7293 can be placed in WAIT or HALT mode thus reducing power consumption. The enhanced instruction set and addressing modes afford real programming potential. In addition to standard 8 bit data management the ST7293 features true bit manipulation, 8x8 unsigned multiplication and indirect addressing modes. The device includes an on-chip oscillator, CPU, ROM, RAM, EEPROM, I/O and one timer with one input capture and two output compare systems.

Figure 2. ST7293 Block Diagram



1.2 PIN DESCRIPTION

V_{DD}. Power supply.

V_{SS}. Ground.

OSCin, OSCout. Oscillator input and output pins. These pins are to be connected to a parallel resonant crystal or ceramic resonator. An external clock source can also be input through OSCin.

$\overline{\text{RESET}}$. The active low input signal forces the initialisation of the MCU. This event is the first priority interrupt. This pin is switched output low when the Watchdog has released. It could be used to reset external peripherals.

$\overline{\text{INT}}$ is the external interrupt signal. Software configuration allows four triggering modes.

ICAP (PC0). Input capture signal going to the TIMER system. This signal, according to a mask option, can be an ICAP pin or PC0 pin. When PC0 is defined as ICAP, the internal pull-up resistor is

not connected.

OCMP1 (PC1). Output compare signal coming from the TIMER system. This output signal, according to a mask option, can be an OCMP1 pin (for output compare 1 of the timer) or PC1 pin. When PC1 is defined as OCMP1, the internal pull-up resistor is not connected.

PA0-PA7, PB0-PB7, PC0-PC5. These 22 lines are standard I/O lines, programmable as either input or output.

– PORT A. 8 Standard I/O lines, bit programmable, accessed through DDRA and DRA Registers. According to a mask option, the outputs can be defined as a standard push-pull output port or as an open drain output port.

– PORT B. 8 Standard I/O lines bit programmable accessed through DDRB and DRB Registers.

– PORT C. 6 Standard I/O lines accessed through DDRC and DRC Registers. According to a mask option, these 6 lines can become 6 falling edge sensitive interrupt lines all linked to a single interrupt vector or 6 standard input ports tied to V_{DD} through an internal pull-up resistor. These negative edge sensitive interrupt lines can wake-up the ST7293 from WAIT or HALT mode.

PIN DESCRIPTION (Continued)

Table 1. ST7293 Pin Configuration

Name	Function	Description	Pin Assignment
$\overline{INT}$	I	Interrupt	1
$\overline{RESET}$	I/O	Reset	2
OSCin	I	Oscillator	3
OSCout	O	Oscillator	4
PB7	I/O	Standard Port (bit programmable)	5
PB6	I/O	Standard Port (bit programmable)	6
PB5	I/O	Standard Port (bit programmable)	7
PB4	I/O	Standard Port (bit programmable)	8
PB3	I/O	Standard Port (bit programmable)	9
PB2	I/O	Standard Port (bit programmable)	10
PB1	I/O	Standard Port (bit programmable)	11
PB0	I/O	Standard Port (bit programmable)	12
PC5	I/O	Standard Port (falling edge interrupt line)	13
PC4	I/O	Standard Port (falling edge interrupt line)	14
PC3	I/O	Standard Port (falling edge interrupt line)	15
PC2	I/O	Standard Port (falling edge interrupt line)	16
PC1 (OCMP1)	I/O	Standard Port (falling edge interrupt line or timer output compare)	17
PC0 (ICAP)	I/O	Standard Port (falling edge interrupt line or timer input capture)	18
PA7	I/O	Standard Port (bit programmable)	19
PA6	I/O	Standard Port (bit programmable)	20
PA5	I/O	Standard Port (bit programmable)	21
PA4	I/O	Standard Port (bit programmable)	22
PA3	I/O	Standard Port (bit programmable)	23
PA2	I/O	Standard Port (bit programmable)	24
PA1	I/O	Standard Port (bit programmable)	25
PA0	I/O	Standard Port (bit programmable)	26
V_{DD}	I/O	Power Supply	27
V_{SS}	I/O	Ground	28

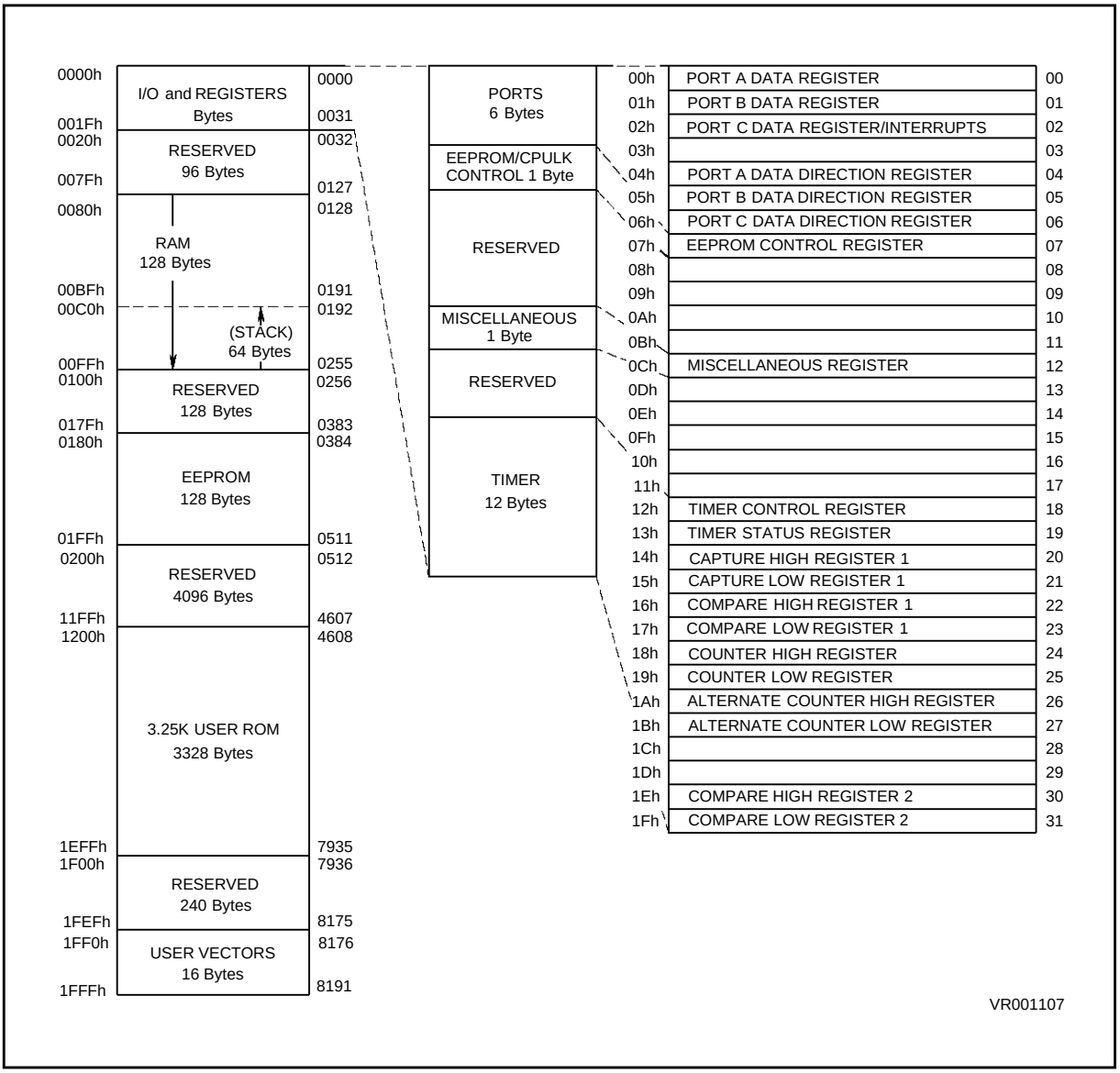
1.3 MEMORY MAP

As shown in Figure 3, the MCU is capable of addressing 8192 bytes of memory and I/O registers. In the ST7293, 3604 of these bytes are user accessible.

The locations consist of 32 bytes of I/O registers (only 20 are used), 128 bytes of RAM, 128 bytes of EEPROM and 3.25Kbytes of user ROM. The RAM space includes 64 bytes for the stack from 0FFh to 0C0h. Programs that only use a small part of the allocated stack locations for interrupts and/or subroutine stacking purpose can use the remaining bytes as standard RAM locations.

The highest address bytes contains the user defined reset and interrupt vectors.

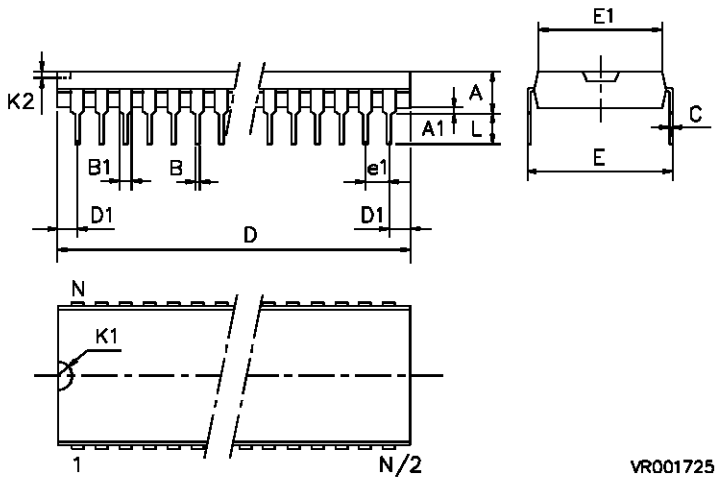
Figure 3. Memory Map



2 GENERAL INFORMATION

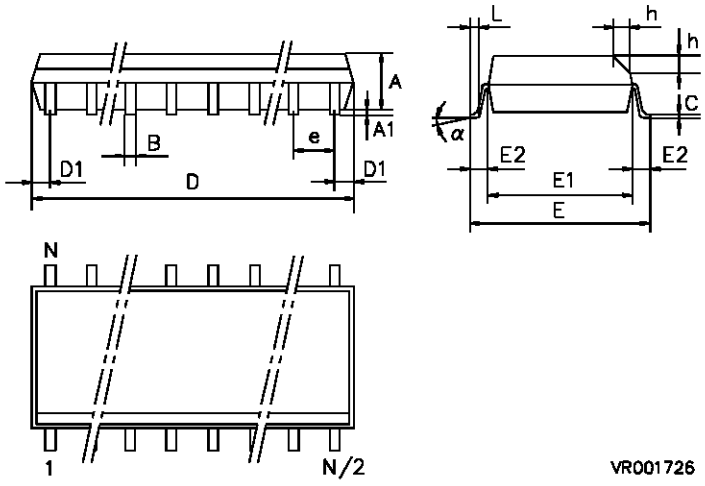
2.1 PACKAGE MECHANICAL DATA

Figure 4. 28-Plastic Dual In Line Package, 600-mil Width



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	2.2		4.8	0.086		0.189
A1	0.51		1.77	0.010		0.069
B	0.38		0.58	0.015		0.023
B1	0.97		1.52	0.055		0.065
C	0.2		0.3	0.008		0.009
D	35.06		36.22	1.400		1.425
D1	–	–	–	–	–	–
E			16.3			0.641
E1		12.9				0.508
K1	–	–	–	–	–	–
K2	–	–	–	–	–	–
L	3.18		4.44	1.25		0.174
e1		2.54			0.10	
	Number of Pins					
N	28					

Figure 5. 28-Lead Small Outline Package, 300-mil Width



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	2.05		2.55	0.081		0.10
A1	0.1		0.3	0.004		.0118
B	0.35		0.49	.0138		.0192
C	0.23		0.32	.0091		.0125
D	17.7		18.1	.6969		.7125
D1	–	–	–	–	–	–
E	10.0		10.65	0.394		0.419
E1	7.40		7.60	.2914		.2992
E2	–	–	–	–	–	–
L	0.40		1.27	0.016		0.050
e1		1.27			0.05	
	Number of Pins					
N	28					

2.2 ST7293 DESCRIPTION

With the following exception, the ST7293 has the same software and hardware features as the ST7294:

1. User ROM: the 3.25K are addressable from 1200h to 1EFFh on the ST7293.
2. Option list: no pull-up option on PORT A and PORT B.

THE READER IS ASKED TO REFER TO THE ST7294 DATASHEET FOR FURTHER DETAILS

2.3 ORDERING INFORMATION

7.2.4 Introduction

The following section describes the approved procedure for transfer of User Program/Data ROM Code to SGS-THOMSON Microelectronics as well as the basis for contractual agreement with respect to mask programmed devices.

7.2.5 Communication of the User ROM Code

To formally communicate the desired Program/ Data ROM contents to SGS-THOMSON Microelectronics, the following must be supplied:

– a file in MOTOROLA S19 FORMAT (on diskette, via electronic mail or by BBS);

– a correctly completed and signed Option List form as shown overleaf.

The User Code must respect the ROM Memory Map for the selected device option.
The User Code must be generated using an approved ST7 assembler. All unused memory locations shall be set to FFh.

7.2.6 Verification and Formal Approval

When SGS-THOMSON Microelectronics receives the User Code file, it will return a copy of the processed file to the Customer. The Customer will then send formal notification to SGS-THOMSON Microelectronics, approving the file contents. This statement and the file copies to which it refers will then form the basis of the contractual agreement between the Customer and SGS-THOMSON Microelectronics and the agreed file will be used to produce the mask for the programmed MCU device.

The SGS-THOMSON Sales Organization will be pleased to provide detailed information relating to the above technical and contractual points.

ORDERING INFORMATION TABLE

Sales Types	ROM Size	Temperature Range	Package
ST7293C3B1	3.25K	0 to +70°C	PDIP28
ST7293C3M1			PSO28
ST7293C3B6		-40 to +85°C	PDIP28
ST7293C3M6			PSO28

ST7293 STANDARD OPTION LIST

Customer Company . . . . . .
Company Address:. . . . . .
Contact Name: . . . . . .
Phone n°: . . . . . .
Fax n°: . . . . . .

SGS-THOMSON Microelectronics references

Package:	[ ] PSO28	[ ] PDIP28
Conditioning (if PSO package):	[ ] Tape & Reel	[ ] Stick (Standard)
Temperature Range:	[ ] 0 to 70°C	[ ] -40 to 85°C

For marking one line with 11 characters maximum is possible
Special Marking [ ] (y/n) "_____"
Authorized characters are letters, digits, ' . ', ' - ', ' / ' and spaces.

OPTIONS:

Watchdog ENABLE MODE	[ ] Software Enable	[ ] Always Enable
Watchdog during WAIT	[ ] Active during WAIT mode	[ ] Suspend during WAIT mode
Enable Wake-up on PORT C	[ ] PORT C 6-bit I/O PORT [ ] PORT C interrupt Wake-up inputs	
Pinout for ICAP (PC0)	[ ] ICAP is bonded on pin 18 [ ] PC0 is bonded on pin 18	
Pinout for OCMP1 (PC1)	[ ] OCMP1 is bonded on pin 17 [ ] PC0 is bonded on pin 17	
PORT A Outputs	[ ] Standard push-pull output PORT [ ] Open Drain output PORT	

Yearly quantity forecast:	[.....] K Units
For a period of	[.....] Years
Preferred production start dates:	[.....] (YY/MM/DD)
Risk order quantity:	[.....]
Agreed A.S.P.	[.....]

Signature . . . . . .
Date . . . . . .

Notes: